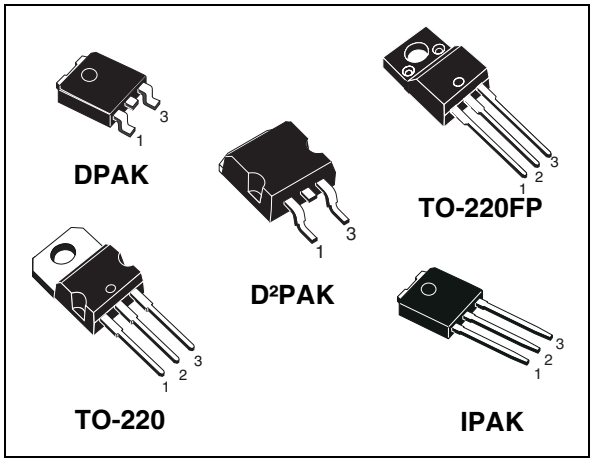
STD5NM60
STB8NM60 - STP8NM60

N-channel 650 V@Tjmax, 0.9 Ω, 8 A MDmesh™ Power MOSFET
TO-220, TO-220FP, D^{2}PAK, DPAK, IPAK

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STD5NM60	650 V	< 1 Ω	5 A	96 W
STD5NM60-1	650 V	< 1 Ω	5 A	96 W
STB8NM60	650 V	< 1 Ω	5 A	100 W
STP8NM60	650 V	< 1 Ω	8 A	100 W
STP8NM60FP	650 V	< 1 Ω	8 A(1)	30 W

- 100% avalanche tested
- HIgh dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the multiple drain process with the company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

Figure 1. Internal schematic diagram

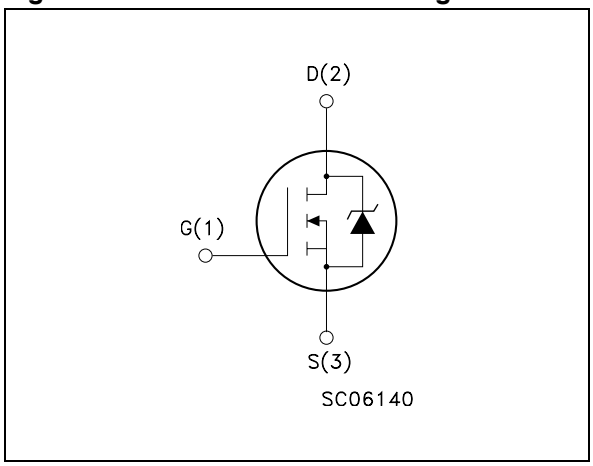


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD5NM60-1	D5NM60	IPAK	Tube
STD5NM60T4	D5NM60	DPAK	Tape & reel
STB8NM60T4	B8NM60	D²PAK	Tape & reel
STP8NM60	P8NM60	TO-220	Tube
STP8NM60FP	P8NM60FP	TO-220FP	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220 D²PAK	TO-220FP	IPAK DPAK	
V_{GS}	Gate-source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25 °C	8	8(1)	5	A
I_D	Drain current (continuous) at T_C=100 °C	5	5 (1)	3.1 (1)	A
I_{DM}(2)	Drain current (pulsed)	32	32 (1)	20 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	100	30	96	W
	Derating factor	0.8	0.24	0.0.4	W/°C
dv/dt(3)	Peak diode recovery voltage slope	15			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	--	2500	--	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 5$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 80%$V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value			Unit
		TO-220 D²PAK	IPAK DPAK	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.25	1.3	4.16	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5			°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D=I_{AS}, V_{DD}=50 V)	200	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} = max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 2.5 A		0.9	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 2.5 A		2.4		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS}=0		400 100 10		pF pF pF
$C_{oss\ eq}$(1).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0 to 480 V		50		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 400 V, I_D = 5 A V_{GS} =10 V		13 5 6	18	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 300 V, I_D= 2.5 A, R_G= 4.7 Ω, V_{GS}=10 V		14 10 23 10		ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD}= 480 V, I_D= 5 A, R_G= 4.7 Ω, V_{GS}=10 V		7 10 17		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				8	A
I_{SDM}(1)	Source-drain current (pulsed)				32	A
V_{SD}(2)	Forward on voltage	I_{SD} = 5A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, V_{DD}=100 V di/dt = 100 A/µs,		300 1.95 13		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, V_{DD} = 100 V di/dt = 100 A/µs, Tj=150 °C		445 3.00 13.5		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220/ D²PAK

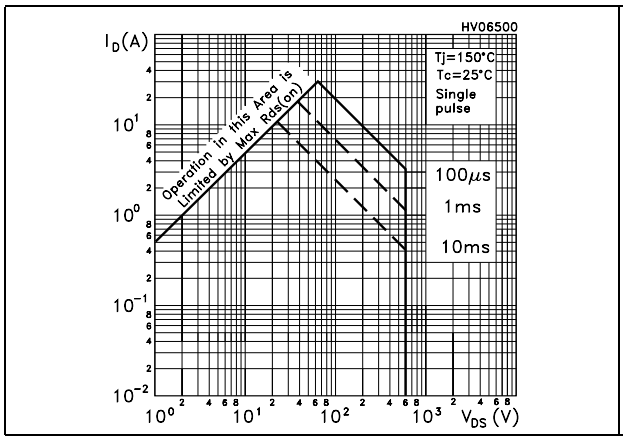


Figure 3. Thermal impedance for TO-220/ D²PAK

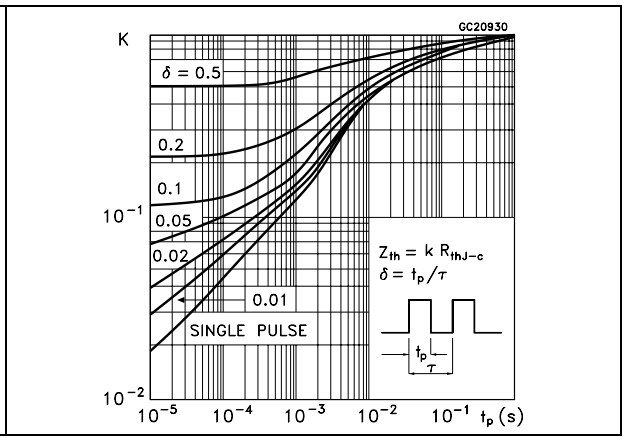


Figure 4. Safe operating area for TO-220FP

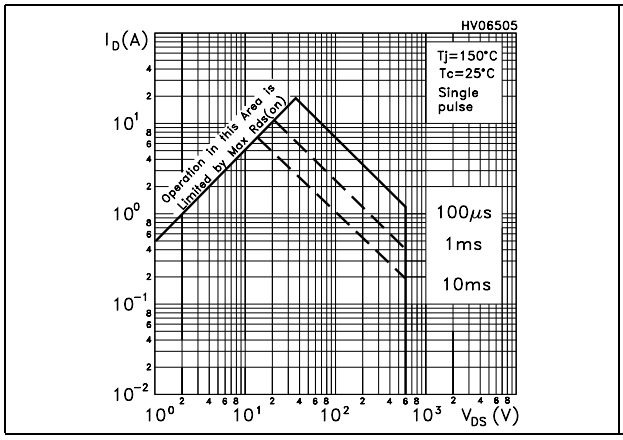


Figure 5. Thermal impedance for TO-220FP

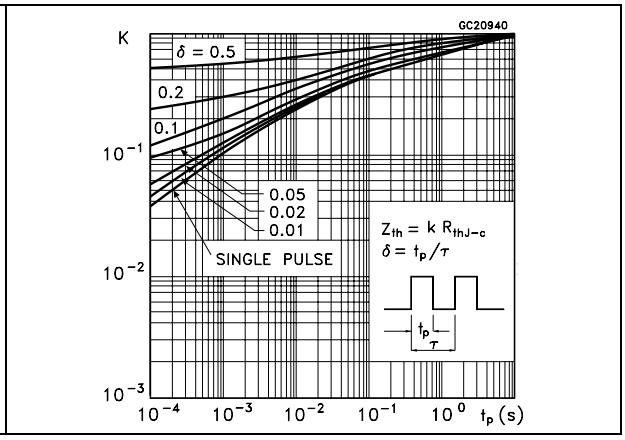


Figure 6. Safe operating area for DPAK/IPAK

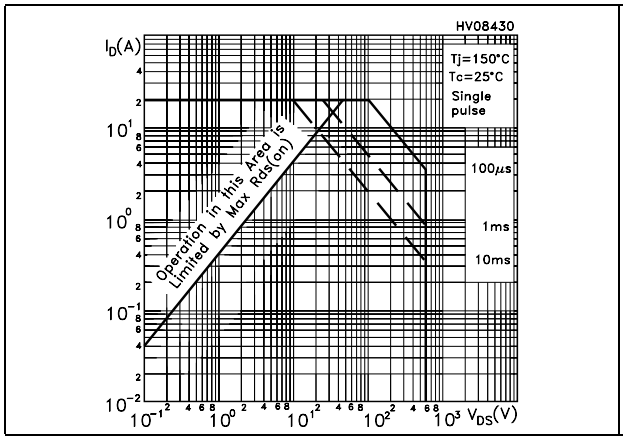


Figure 7. Thermal impedance for DPAK/IPAK