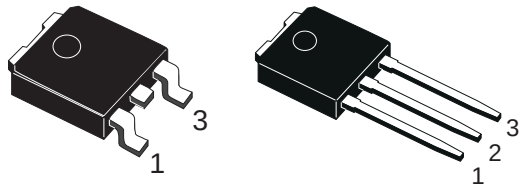
STD5NM50
STD5NM50-1

N-CHANNEL 500V - 0.7Ω - 7.5A DPAK/IPAK
MDmesh™Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD5NM50	500V	<0.8Ω	7.5 A
STD5NM50-1	500V	<0.8Ω	7.5 A

- TYPICAL R_{DS}(on) = 0.7Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS



DPAK
TO-252

IPAK
TO-251
(Add Suffix "-1")

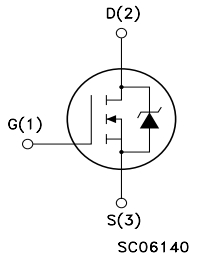
DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuous) at T_C = 25°C	7.5	A
I_D	Drain Current (continuous) at T_C = 100°C	4.7	A
I_{DM} (•)	Drain Current (pulsed)	30	A
P_{TOT}	Total Dissipation at T_C = 25°C	100	W
	Derating Factor	0.8	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T_{stg}	Storage Temperature	– 55 to 150	°C
T_j	Max. Operating Junction Temperature		

(•)Pulse width limited by safe operating area

(1) $I_{SD} \leq$ 5A, di/dt ≤ 400A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.25	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 2.5A		0.7	0.8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 25V_x, I_D = 2.5A		3.5		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		415		pF
C_{oss}	Output Capacitance			88		pF
C_{rss}	Reverse Transfer Capacitance			12		pF
$C_{oss\ eq.}$ (2)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		50		pF
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

ELECTRICAL CHARACTERISTICS (CONTINUED)
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 250V, I_D = 2.5A R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		16		ns
t_r	Rise Time			8		ns
Q_g	Total Gate Charge	V_{DD} = 400V, I_D = 7.5A V_{GS} = 10V		13		nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			6		nC

SWITCHING OFF

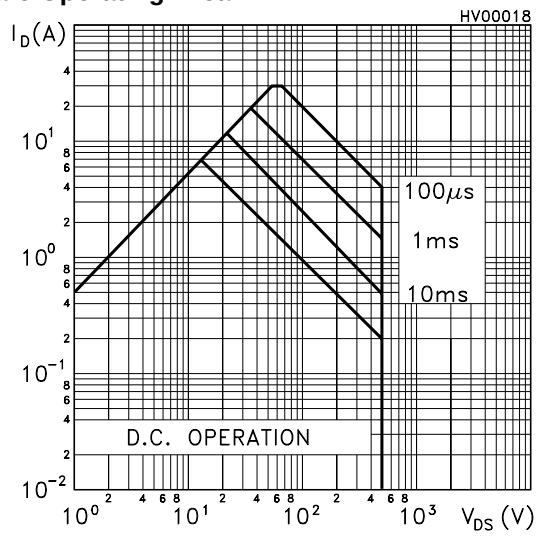
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 400V, I_D = 5A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		14		ns
t_f	Fall Time			6		ns
t_c	Cross-over Time			13		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				7.5	A
I_{SDM} (2)	Source-drain Current (pulsed)				30	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 7.5A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 5A, di/dt = 100A/µs, V_{DD} = 100V, T_j = 25°C (see test circuit, Figure 5)		185		ns
Q_{rr}	Reverse Recovery Charge			1.1		µC
I_{RRM}	Reverse Recovery Current			11.5		A
t_{rr}	Reverse Recovery Time	I_{SD} = 5A, di/dt = 100A/µs, V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		270		ns
Q_{rr}	Reverse Recovery Charge			1.6		µC
I_{RRM}	Reverse Recovery Current			12		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area



Thermal Impedance