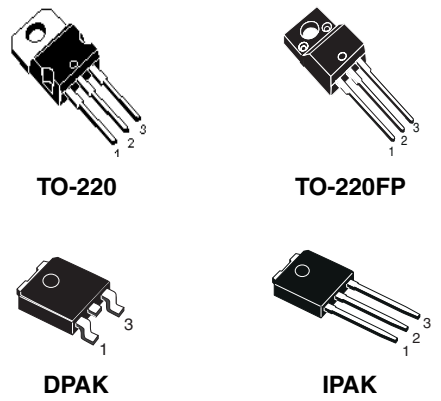
STP4NK80Z - STP4NK80ZFP
STD4NK80Z - STD4NK80Z-1

N-channel 800V - 3Ω - 3A - TO-220/TO-220FP/DPAK/IPAK
Zener - Protected SuperMESH™ MOSFET

General features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STP4NK80Z	800 V	< 3.5 Ω	3 A
STP4NK80ZFP	800 V	< 3.5 Ω	3 A
STD4NK80Z	800 V	< 3.5 Ω	3 A
STD4NK80Z-1	800 V	< 3.5 Ω	3 A

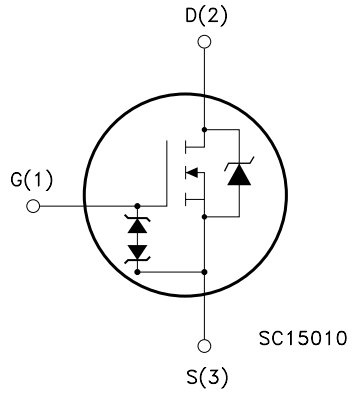
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP4NK80Z	P4NK80Z	TO-220	Tube
STP4NK80ZFP	P4NK80ZFP	TO-220FP	Tube
STD4NK80ZT4	D4NK80Z	DPAK	Tape & reel
STD4NK80Z-1	D4NK80Z	IPAK	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/DPAK/ IPAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	800		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	3	3 (1)	A
I_D	Drain current (continuous) at T_C=100°C	1.89	1.89 (1)	A
I_{DM}(2)	Drain current (pulsed)	12	12 (1)	A
P_{TOT}	Total dissipation at T_C = 25°C	80	25	W
	Derating factor	0.64	0.21	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5KΩ)	3000		V
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; T_c= 25°C)	-	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤4A, di/dt ≤200A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j ≤T_{JMAX}.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	DPAK IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.56	5	1.56	°C/W
R_{thj-a}	Thermal resistance junction-ambient max	62.5		100	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	3	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	190	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (Open Drain)	30			V

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, Tc = 125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{GS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 1.5 A		3	3.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 1.5A		2.9		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		575 67 13		pF pF pF
C_{osseq} (2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 400V		60		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Off-voltage rise time Fall time	V_{DD}=400 V, I_D= 1.5 A, R_G=4.7Ω, V_{GS}=10V		13 12 35 32		ns ns ns ns
$t_{r(Voff)}$ t_r t_c	Off-voltage rise time Fall time Cross-over time	V_{DD}=640 V, I_D= 3 A, R_G=4.7Ω, V_{GS}=10V		18 7.5 25		ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=640V, I_D = 3 A V_{GS} =10V		22.5 4.2 11.3		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				3 12	A A
V_{SD}(2)	Forward on voltage	I_{SD}= 3 A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 3 A, di/dt = 100A/µs, V_{DD}=80 V, Tj=150°C		400 1520 7.6		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/DPAK/IPAK

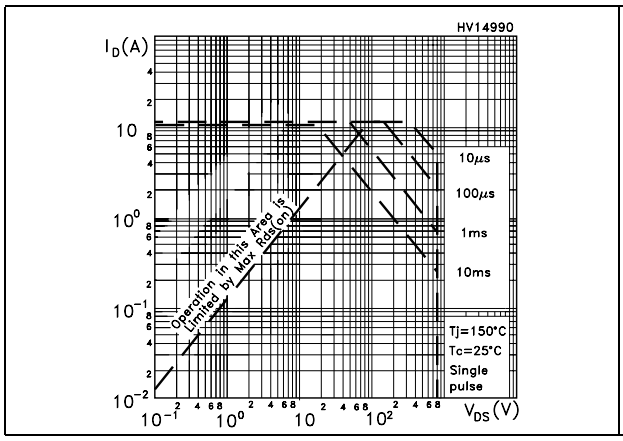


Figure 2. Thermal impedance for TO-220/DPAK/IPAK

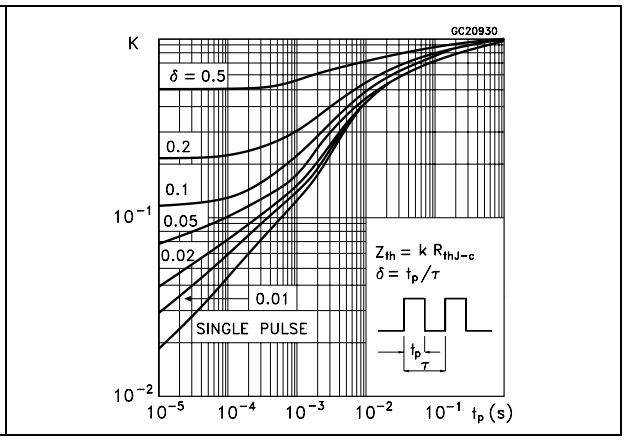


Figure 3. Safe operating area for TO-220FP

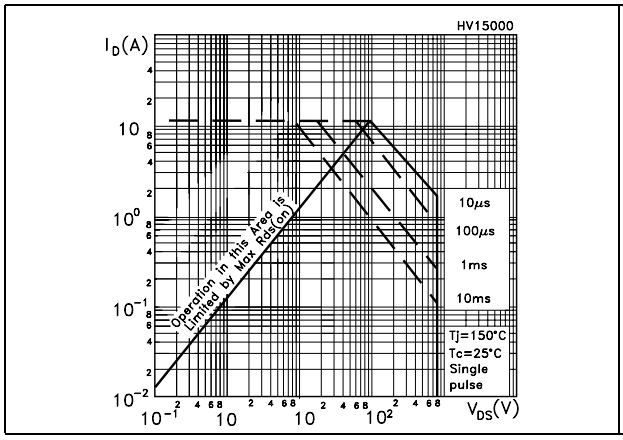


Figure 4. Thermal impedance for TO-220FP

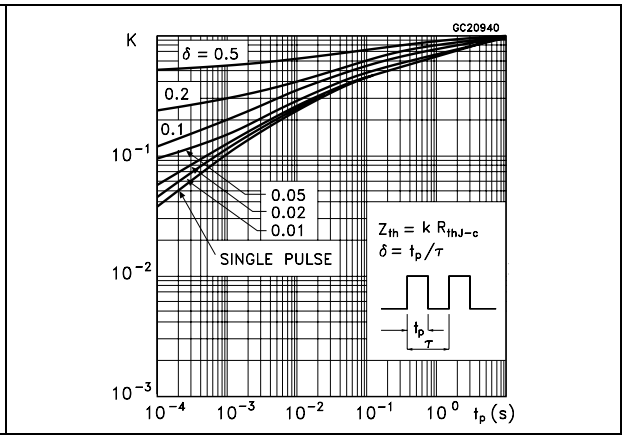


Figure 5. Output characterisics

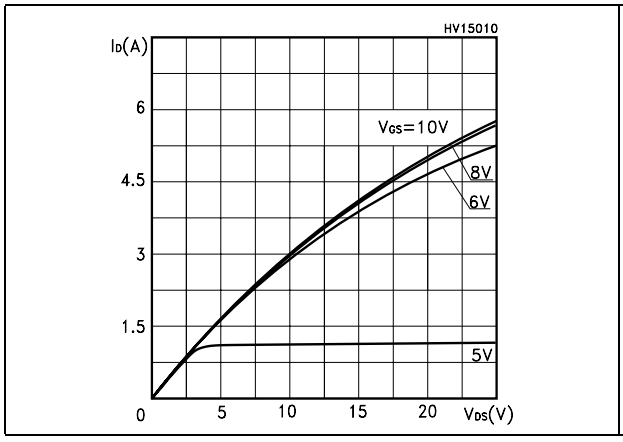


Figure 6. Transfer characteristics