



STB4NK60Z, STB4NK60Z-1, STD4NK60Z STD4NK60Z-1, STP4NK60Z, STP4NK60ZFP

N-channel 600 V, 1.76 Ω , 4 A SuperMESH™ Power MOSFET
in DPAK, D²PAK, IPAK, I²PAK, TO-220, TO-220FP

Features

| Type | V _{DSS} | R _{DS(on)} max | P _W | I _D |
|-------------|------------------|-------------------------|----------------|----------------|
| STB4NK60Z | 600 V | < 2 Ω | 70 W | 4 A |
| STB4NK60Z-1 | 600 V | < 2 Ω | 70 W | 4 A |
| STD4NK60Z | 600 V | < 2 Ω | 70 W | 4 A |
| STD4NK60Z-1 | 600 V | < 2 Ω | 70 W | 4 A |
| STP4NK60Z | 600 V | < 2 Ω | 70 W | 4 A |
| STP4NK60ZFP | 600 V | < 2 Ω | 25 W | 4 A |

- 100% avalanche tested
- Very low intrinsic capacitances

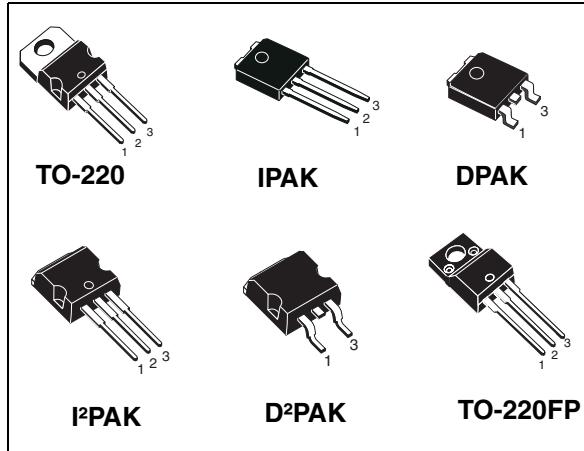


Figure 1. Internal schematic diagram

Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

| Order codes | Marking | Package | Packaging |
|-------------|-----------|--------------------|---------------|
| STB4NK60Z | B4NK60Z | D ² PAK | Tape and reel |
| STB4NK60Z-1 | B4NK60Z | I ² PAK | Tube |
| STD4NK60Z | D4NK60Z | DPAK | Tape and reel |
| STD4NK60Z-1 | D4NK60Z | IPAK | Tube |
| STP4NK60Z | P4NK60Z | TO-220 | Tube |
| STP4NK60ZFP | P4NK60ZFP | TO-220FP | Tube |

1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | | Unit |
|--------------------------------|---|---|--------------------|------|
| | | TO-220 - D ² PAK DPAK-IPAK-I ² PAK | TO-220FP | |
| V _{DS} | Drain-source voltage (V _{GS} = 0) | 600 | | V |
| V _{GS} | Gate- source voltage | ± 30 | | V |
| I _D | Drain current (continuous) at T _C = 25 °C | 4 | 4 ⁽¹⁾ | A |
| I _D | Drain current (continuous) at T _C = 100 °C | 2.5 | 2.5 ⁽¹⁾ | A |
| I _{DM} ⁽²⁾ | Drain current (pulsed) | 16 | 16 ⁽¹⁾ | A |
| P _{TOT} | Total dissipation at T _C = 25 °C | 70 | 25 | W |
| | Derating factor | 0.56 | 0.2 | W/°C |
| V _{ESD(G-S)} | Gate source ESD(HBM-C=100 pF, R=1.5 kΩ) | 3000 | | V |
| dv/dt ⁽³⁾ | Peak diode recovery voltage slope | 4.5 | | V/ns |
| V _{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C = 25 °C) | - | 2500 | V |
| T _{stg} | Storage temperature | -55 to 150 | | °C |
| T _j | Max operating junction temperature | 150 | | °C |

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}.

Table 3. Thermal data

| Symbol | Parameter | Value | | | Unit |
|-----------------------|--|--|--------------|----------|------|
| | | TO-220 D ² PAK I ² PAK | DPAK IPAK | TO-220FP | |
| R _{thj-case} | Thermal resistance junction-case max | 1.78 | | 5 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient max | 62.5 | 100 | 62.5 | °C/W |
| T _I | Maximum lead temperature for soldering purpose | 300 | | | °C |

Table 4. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|---|-------|------|
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max) | 4 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25^\circ C$, $I_D=I_{AR}$, $V_{DD}= 50 V$) | 120 | mJ |

2 Electrical characteristics

($T_{CASE} = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|--|---|------|------|----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1 \text{ mA}, V_{GS} = 0$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ\text{C}$ | | | 1 50 | μA μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20 \text{ V}$ | | | ± 10 | μA |
| $V_{GS(\text{th})}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 50 \mu\text{A}$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(\text{on})}$ | Static drain-source on resistance | $V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$ | | 1.76 | 2 | Ω |

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|--|------|-------------------------|------|----------------------|
| $g_{fs}^{(1)}$ | Forward transconductance | $V_{DS} = 15 \text{ V}, I_D = 2 \text{ A}$ | | 3 | | S |
| C_{iss} C_{oss} C_{rss} | Input capacitance Output capacitance Reverse transfer capacitance | $V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$ | | 510 67 13 | | pF pF pF |
| $C_{oss \text{ eq.}}^{(2)}$ | Equivalent output capacitance | $V_{DS} = 0, V_{DS} = 0 \text{ to } 480 \text{ V}$ | | 38.5 | | pF |
| $t_{d(on)}$ t_r $t_{d(off)}$ t_f | Turn-on delay time Rise time Turn-off delay time Fall time | $V_{DD} = 300 \text{ V}, I_D = 2 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ | | 12 9.5 29 16.5 | | ns ns ns ns |
| $t_{r(Voff)}$ t_r t_c | Off-voltage rise time Fall time Cross-over time | $V_{DD} = 480 \text{ V}, I_D = 4 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ | | 12 12 19.5 | | ns ns ns |
| Q_g Q_{gs} Q_{gd} | Total gate charge Gate-source charge Gate-drain charge | $V_{DD} = 480 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}$ | | 18.8 3.8 9.8 | 26 | nC nC nC |

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|------|
| I_{SD} | Source-drain current | | | | 4 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | | | 16 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 4 \text{ A}, V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 4 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ | | 400 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 24 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ | | 1700 | | nC |
| I_{RRM} | Reverse recovery current | | | 8.5 | | A |

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|-------------------------------|---|------|------|------|------|
| BV_{GSO} | Gate-source breakdown voltage | $I_{GS} = \pm 1 \text{ mA} (\text{open drain})$ | 30 | | | V |

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / DPAK / IPAK / D²PAK / I²PAK

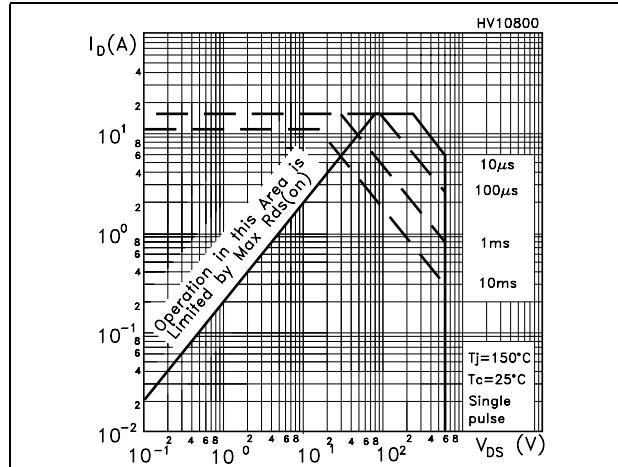


Figure 3. Thermal impedance for TO-220 / DPAK / IPAK / D²PAK / I²PAK

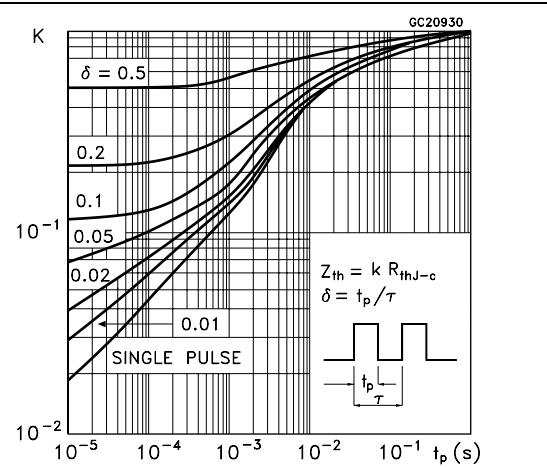


Figure 4. Safe operating area for TO-220FP

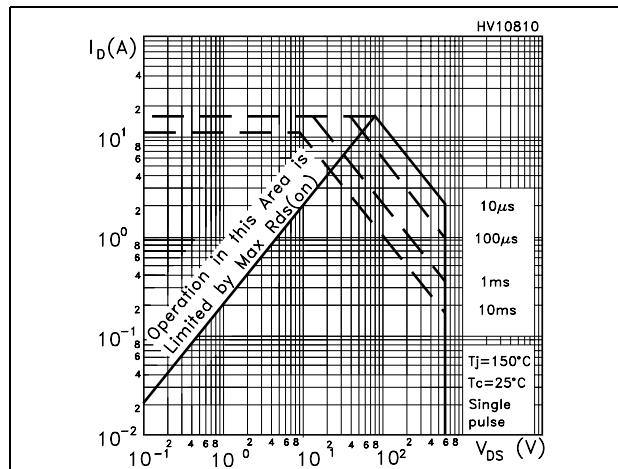


Figure 5. Thermal impedance for TO-220FP

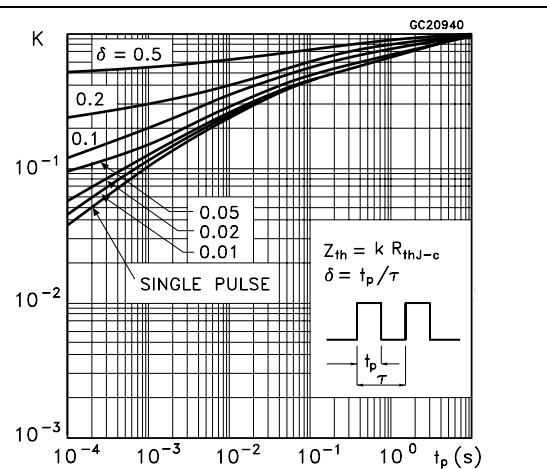


Figure 6. Output characteristics

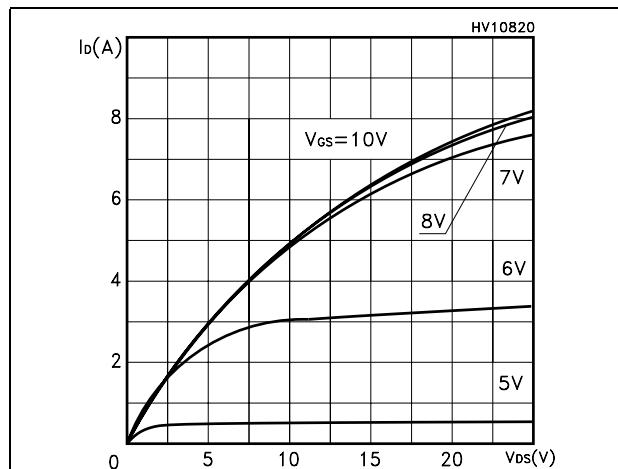


Figure 7. Transfer characteristics

