STD3NK90Z, STP3NK90Z, STP3NK90ZFP

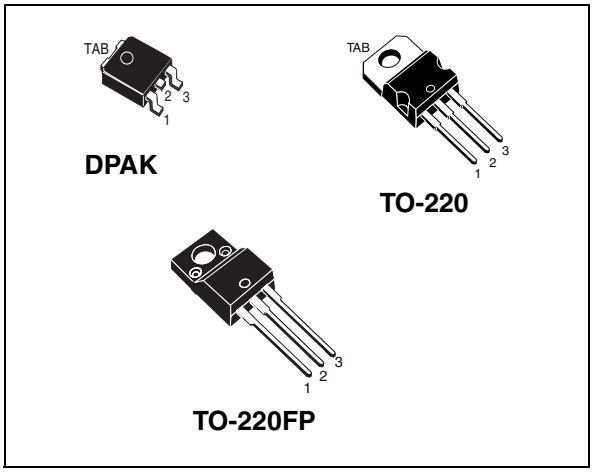
N-channel 900 V, 4.1 Ω typ., 3 A Zener-protected SuperMESH™ Power MOSFET in DPAK, TO-220 and TO-220FP packages

Datasheet – production data

Features

Order codes	V_{DS}	$R_{DS(on)}$	I_D	P_{TOT}
STD3NK90ZT4	900 V	4.8 Ω	3 A	90 W
STP3NK90Z				
STP3NK90ZFP				25 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very good manufacturing repeatability
- Very low intrinsic capacitances



Applications

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

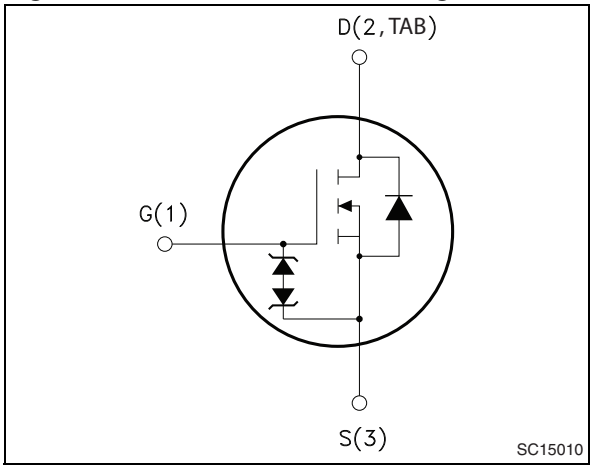


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD3NK90ZT4	D3NK90Z	DPAK	Tape and reel
STP3NK90Z	P3NK90Z	TO-220	Tube
STP3NK90ZFP	P3NK90ZFP	TO-220FP	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220	TO-220FP	
V_{DS}	Drain-source voltage	900		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	3	3 (1)	A
I_D	Drain current (continuous) at T_C = 100°C	1.89	1.89 (1)	A
I_{DM} (2)	Drain current (pulsed)	12	12 (1)	A
P_{TOT}	Total dissipation at T_C = 25°C	90	25	W
	Derating factor	0.72	0.2	W/°C
E_{SD}	Gate-source human body model (R=1,5 kΩ, C=100 pF)	4		kV
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all threeleads to external heat sink (t=1s;Tc=25°C)		2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 3A$, $di/dt \leq 200A/\mu s$, V_{DD} =80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	DPAK	TO-220	TO-220FP	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.38		5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max		62.5		°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	50			°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	3	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AR}, V_{DD}= 50V)	180	mJ

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	900			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 900 V V_{DS} = 900 V, T_j=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V, V_{DS} = 0			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 1.5 A		4.1	4.8	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15 V, I_D = 1.5 A	-	2.7	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	590 63 13	-	pF pF pF
$C_{oss\ eq}$ (2)	Equivalent ouput capacitance	V_{GS}=0, V_{DS} =0 V to 400 V	-	34	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=720 V, I_D = 3 A V_{GS} =10 V *see*	-	22.7 4.2 12	-	nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq}$. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=450 V, I_D= 1.5 A, R_G=4.7 Ω, V_{GS}=10 V	-	18 7	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=720 V, I_D= 1.5 A, R_G=4.7 Ω, V_{GS}=10 V	-	45 18	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		3 12	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 3 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 3 A, di/dt = 100A/µs, V_{DD}=40 V, T_j=150°C	-	510 2.2 8.7		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}=± 1 mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and TO-220

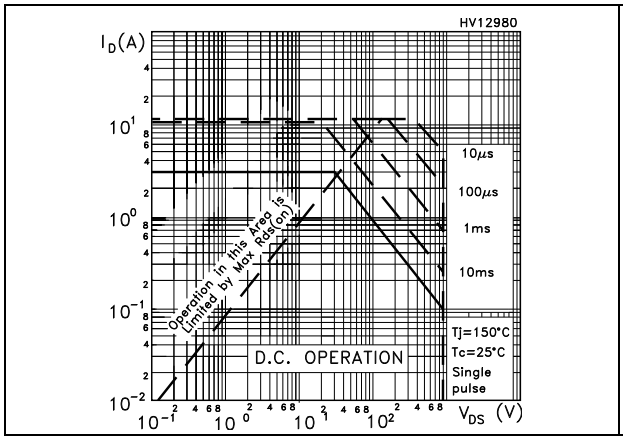


Figure 3. Thermal impedance for DPAK and TO-220

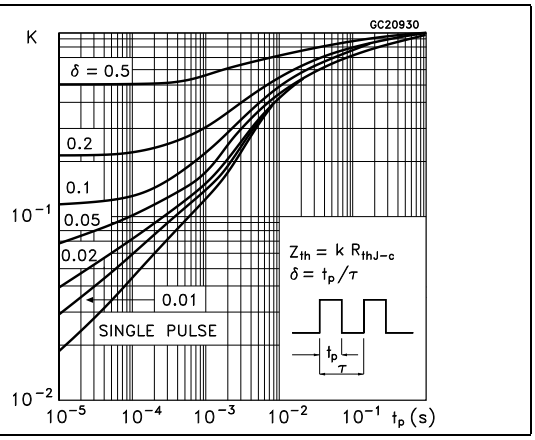


Figure 4. Safe operating area for TO-220FP

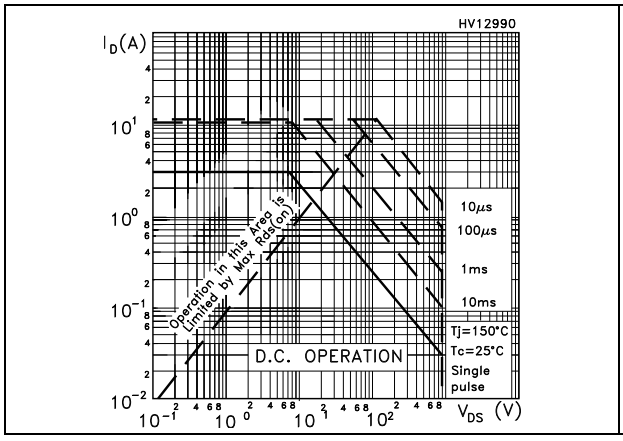


Figure 5. Thermal impedance for TO-220FP

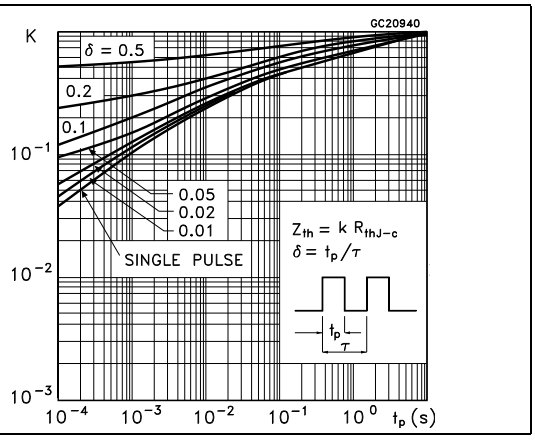


Figure 6. Output characterisics

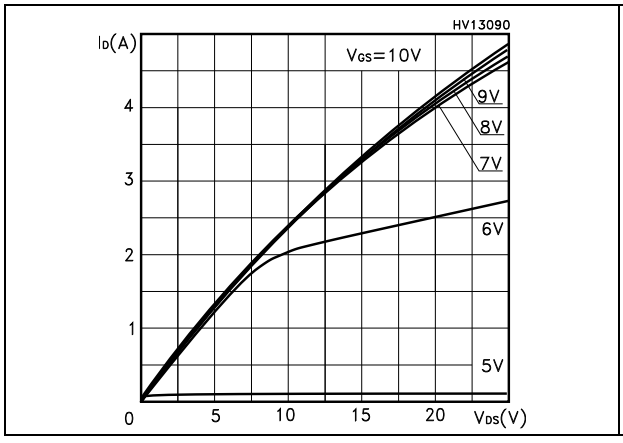
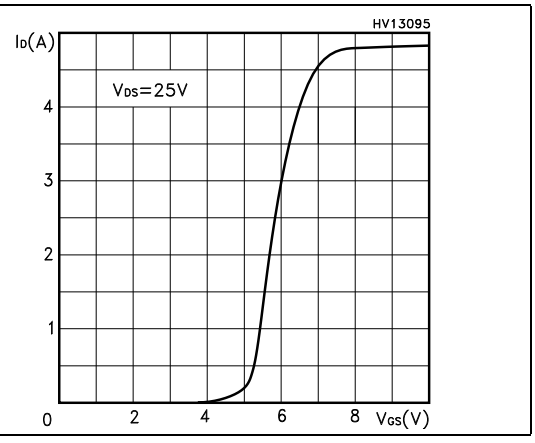



Figure 7. Transfer characteristics