

STB3N62K3, STD3N62K3, STF3N62K3 STP3N62K3, STU3N62K3

N-channel 620 V, 2.2 Ω, 2.7 A SuperMESH3™ Power MOSFET
D²PAK, DPAK, TO-220FP, TO-220, IPAK

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _D
STB3N62K3	620 V	< 2.5 Ω	2.7 A	45 W
STD3N62K3	620 V	< 2.5 Ω	2.7 A	45 W
STF3N62K3	620 V	< 2.5 Ω	2.7 A ⁽¹⁾	20 W
STP3N62K3	620 V	< 2.5 Ω	2.7 A	45 W
STU3N62K3	620 V	< 2.5 Ω	2.7 A	45 W

1. Limited by package
- 100% avalanche tested
 - Extremely high dv/dt capability
 - Very low intrinsic capacitances
 - Improved diode reverse recovery characteristics
 - Zener-protected

Application

- Switching applications

Description

The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimization of the vertical structure. In addition to reducing on-resistance significantly versus previous generation, special attention has been taken to ensure a very good dv/dt capability and higher margin in breakdown voltage for the most demanding application.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB3N62K3	3N62K3	D ² PAK	Tape and reel
STD3N62K3	3N62K3	DPAK	Tape and reel
STF3N62K3	3N62K3	TO-220FP	Tube
STP3N62K3	3N62K3	TO-220	Tube
STU3N62K3	3N62K3	IPAK	Tube

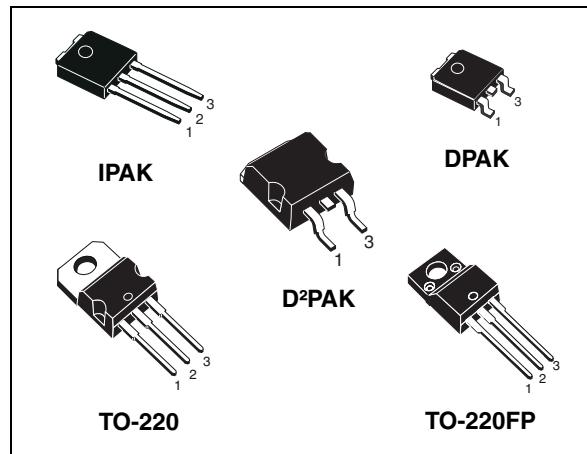


Figure 1. Internal schematic diagram

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit		
		TO-220 D ² PAK	DPAK IPAK	TO-220FP			
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	620			V		
V_{GS}	Gate- source voltage	± 30			V		
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	2.7		2.7 ⁽¹⁾	A		
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.7		1.7 ⁽¹⁾	A		
I_{DM} ⁽²⁾	Drain current (pulsed)	10.8		10.8 ⁽¹⁾	A		
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	45		20	W		
	Derating factor	0.36		0.16	W/ $^\circ\text{C}$		
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100 pF, $R = 1.5 \text{ k}\Omega$)	2500			V		
dv/dt ⁽³⁾	Peak diode recovery voltage slope	9			V/ns		
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1 \text{ s}$; $T_C = 25^\circ\text{C}$)	--	2500		V		
T_{stg}	Storage temperature	-55 to 150			$^\circ\text{C}$		
T_j	Max. operating junction temperature	150			$^\circ\text{C}$		

1. Limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 2.7 \text{ A}$, $dI/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	D ² PAK	DPAK	IPAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.78			6.25	$^\circ\text{C/W}$	
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	50		--	$^\circ\text{C/W}$	
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		100		62.5	$^\circ\text{C/W}$
T_I	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$		

Electrical ratings**STB3N62K3, STD3N62K3, STF3N62K3, STP3N62K3, STU3N62K3****Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.7	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	100	mJ

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	620			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ\text{C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50 \mu\text{A}$	3	3.75	4.5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 1.4 \text{ A}$		2.2	2.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	$V_{DS} = 15 \text{ V}, I_D = 1.4 \text{ A}$	-	2.1	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	385 55 6	-	pF pF pF
$C_{oss \text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0 \text{ to } 496 \text{ V}$	-	32.3	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	10	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 496 \text{ V}, I_D = 2.7 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	13 2.5 7.5	-	nC nC nC

1. $C_{oss \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(\text{on})}$ t_r	Turn-on delay time Rise time	$V_{DD} = 310 \text{ V}, I_D = 1.7 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	9 6.8	-	ns ns
$t_{d(\text{off})}$ t_f	Turn-off-delay time Fall time			22 15.6	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				10.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.7 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.7 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$		190		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see)	-	825		nC
I_{RRM}	Reverse recovery current			9		A
t_{rr}	Reverse recovery time	$I_{SD} = 2.7 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$		255		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	1100		nC
I_{RRM}	Reverse recovery current			10		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, IPAK, DPAK, D²PAK

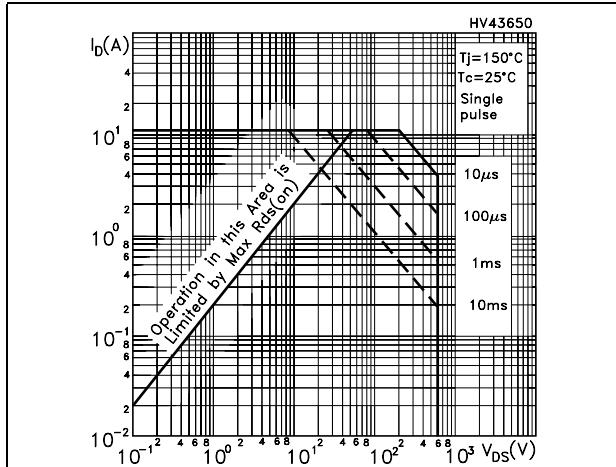


Figure 3. Thermal impedance for TO-220, IPAK, DPAK, D²PAK

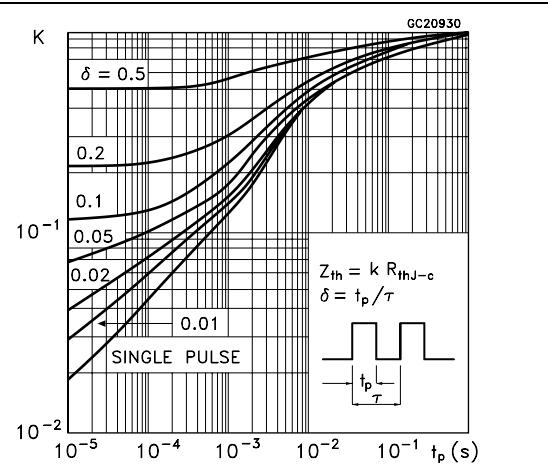


Figure 4. Safe operating area for TO-220FP

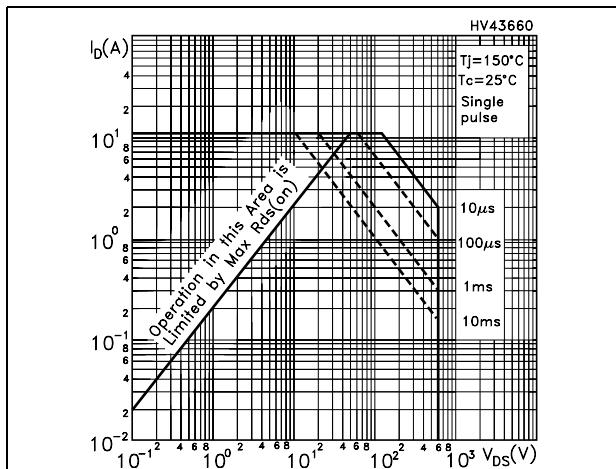


Figure 5. Thermal impedance for TO-220FP

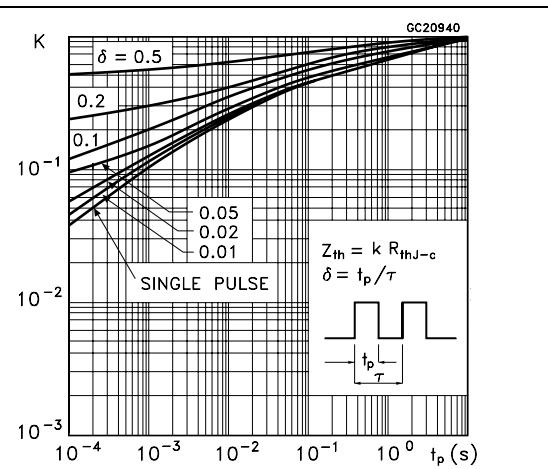


Figure 6. Output characteristics

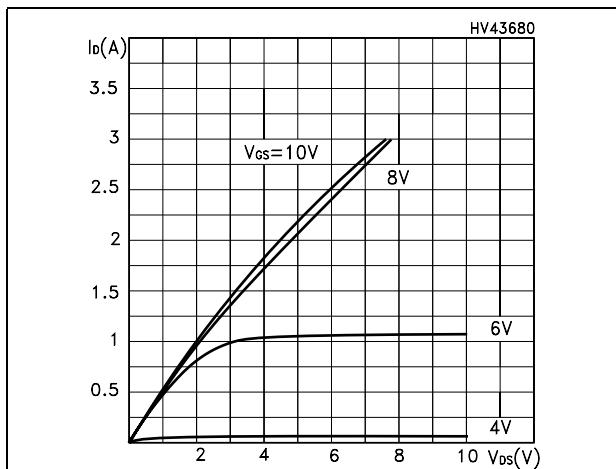


Figure 7. Transfer characteristics

