# STD2NK70Z - STD2NK70Z-1

## N-CHANNEL 700 V - 6 Ω - 1.6 A DPAK/IPAK Zener-Protected SuperMESH™ MOSFET

**Table 1: General Features**

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ | Pw |
|---|---|---|---|---|
| STD2NK70Z | 700 V | 7 Ω | 1.6 A | 45 W |
| STD2NK70Z-1 | 700 V | 7 Ω | 1.6 A | 45 W |

- TYPICAL $R_{DS}$(on) = 6 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

**Figure 1: Package**

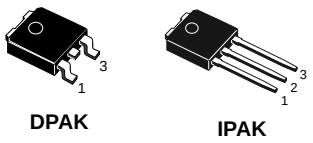
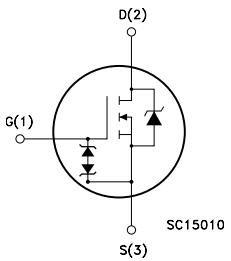



**Figure 2: Internal Schematic Diagram**




### DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high vltage MOS-FETs including revolutionary MDmesh™ products.

### APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT
- FLYBACK CONFIGURATION FOR BATTERY CHARGER

**Table 2: Order Codes**

| Sales Type | Marking | Package | Packaging |
|---|---|---|---|
| STD2NK70ZT4 | D2NK70Z | DPAK | TAPE & REEL |
| STD2NK70Z-1 | D2NK70Z | IPAK | TUBE |

**Table 3: Absolute Maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 700 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 KΩ) | 700 | V |
| $V_{GS}$ | Gate- source Voltage | ± 30 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C | 1.6 | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 1 | A |
| $I_{DM}$(*) | Drain Current (pulsed) | 6.4 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 45 | W |
| | Derating Factor | 0.36 | W/°C |
| $V_{ESD(G-S)}$ | Gate source ESD (HBM-C = 100pF, R = 1.5 KΩ) | 2000 | V |
| dv/dt (1) | Peak Diode Recovery voltage slope | 4.5 | V/ns |
| $T_{stg}$ | Storage Temperature | -55 to 150 | °C |
| $T_j$ | Max. Operating Junction Temperature | | |

(*) Pulse width limited by safe operating area
(1) $I_{SD} \leq$ 1.6 A, di/dt $\leq$ 200 A/µs, VDD $\leq$ $V_{(BR)DSS}$

**Table 4: Thermal Data**

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 2.78 | °C/W |
| Rthj-amb<br>$T_l$ | Thermal Resistance Junction-ambient Max<br>Maximum Lead Temperature For Soldering Purpose | 100<br>300 | °C/W<br>°C |

**Table 5: Avalanche Characteristics**

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 1.6 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 110 | mJ |

**Table 6: Gate-Source Zener Diode**

| Symbol | Parameter | Test Condition | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $BV_{GSO}$ | Gate-Source Breakdown Voltage | Igs= ± 1mA (Open Drain) | 30 | | | A |

## PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**TABLE 7: ELECTRICAL CHARACTERISTICS** ($T_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)

**On /Off**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 700 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating, $T_C$ = 125°C | | | 1<br>50 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ± 10 | µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 50 µA | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 0.8 A | | 6 | 7 | Ω |

**Table 8: Dynamic**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS}$ = 15 V,<br>$I_D$ = 0.8 A | | 1.4 | | S |
| $C_{oss\ eq.}$(3) | Equivalent Output Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 560 V | | 17 | | |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 | | 280<br>35<br>6.5 | | pF<br>pF<br>pF |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on Delay Time<br>Rise Time<br>Turn-off-Delay Time<br>Fall Time | $V_{DD}$ = 350 V, $I_D$ = 0.8 A,<br>$R_G$ = 4.7 Ω, $V_{GS}$ = 10 V<br>(see Figure 17) | | 7<br>17<br>20<br>35 | | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 560 V, $I_D$ = 0.8 A,<br>$V_{GS}$ = 10 V<br>(see Figure 20) | | 11.4<br>2<br>6.8 | 15 | nC<br>nC<br>nC |

**Table 9: Source Drain Diode**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (2) | Source-drain Current<br>Source-drain Current (pulsed) | | | | 1.6<br>6.4 | A<br>A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 1.6 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 1.6, di/dt = 100 A/µs<br>$V_{DD}$ =50 V, $T_j$ = 25°C<br>(see Figure 18) | | 334<br>918<br>5.5 | | ns<br>µC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 1.6, di/dt = 100 A/µs<br>$V_{DD}$ = 50 V, $T_j$ = 150°C<br>(see Figure 18) | | 350<br>1050<br>6 | | ns<br>µC<br>A |

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
(2) Pulse width limited by safe operating area
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Figure 3: Safe Operating Area**

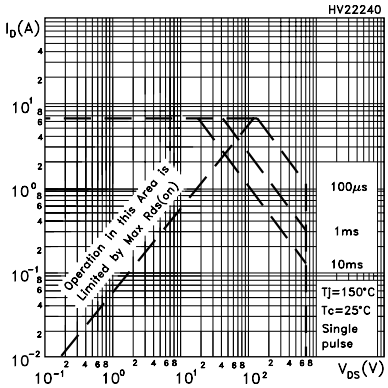



**Figure 4: Output Characteristics**

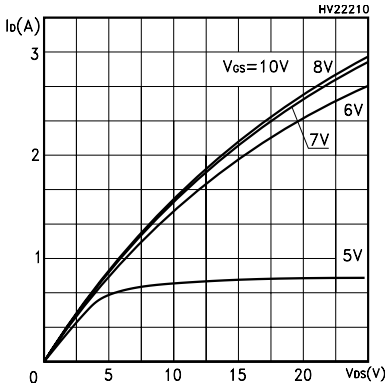



**Figure 5: Transconductance**

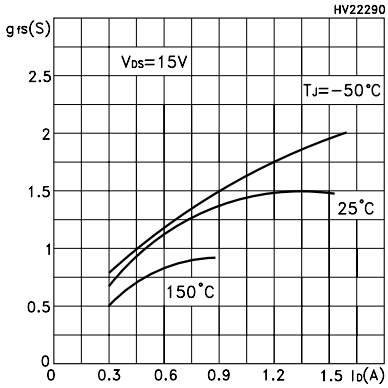



**Figure 6: Thermal Impedance**

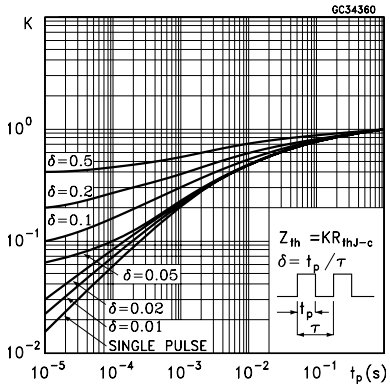
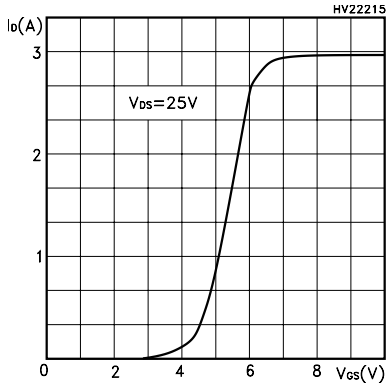



**Figure 7: Transfer Characteristics**



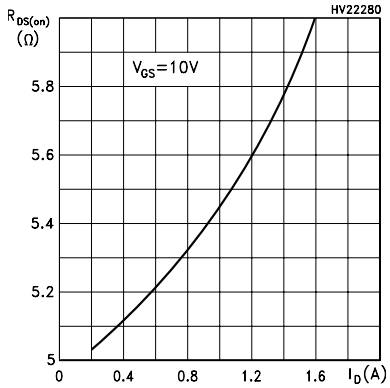


**Figure 8: Static Drain-source On Resistance**