STF2NK60Z - STQ2NK60ZR-AP
STP2NK60Z - STD2NK60Z-1

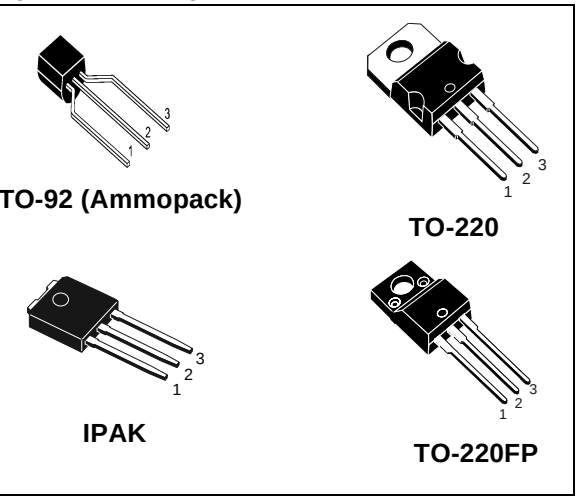
N-CHANNEL 600V - 7.2Ω - 1.4A TO-220/TO-220FP/TO-92/IPAK
Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STF2NK60Z	600 V	< 8 Ω	1.4 A	20
STQ2NK60ZR-AP	600 V	< 8 Ω	0.4 A	3 W
STP2NK60Z	600 V	< 8 Ω	1.4 A	45 W
STD2NK60Z-1	600 V	< 8 Ω	1.4 A	45 W

- TYPICAL $R_{DS}(on)$ = 7.2 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

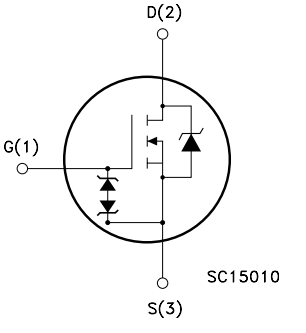
Figure 1: Package



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOS-FETs including revolutionary MDmesh™ products.

Figure 2: Internal Schematic Diagram



APPLICATIONS

- LOW POWER BATTERY CHARGERS
- SWITH MODE LOW POWER SUPPLIES(SMPS)
- LOW POWER, BALLAST, CFL (COMPACT FLUORESCENT LAMPS)

Table 2: Order Codes

Part Number	Marking	Package	Packaging
STQ2NK60ZR-AP	Q2NK60ZR	TO-92	AMMOPAK
STP2NK60Z	P2NK60Z	TO-220	TUBE
STD2NK60Z-1	D2NK60Z	IPAK	TUBE
STF2NK60Z	F2NK60Z	TO-220FP	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value			Unit
		TO-220 / IPAK	TO-92	TO-220FP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600			V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600			V
V_{GS}	Gate- source Voltage	± 30			V
I_D	Drain Current (continuous) at T_C = 25°C	1.4	0.4	1.4 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	0.77	0.25	0.77 (*)	A
I_{DM} (•)	Drain Current (pulsed)	5.6	1.6	5.6 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	45	3	20	W
	Derating Factor	0.36	0.025	0.16	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	1500			V
V_{ISO}	Insulation Withstand Voltage (DC)			2500	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(•) Pulse width limited by safe operating area
(1) $I_{SD} \leq 1.4A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$
(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220/IPAK	TO-220FP	TO-92	Unit
Rthj-case	Thermal Resistance Junction-case Max	2.77	6.25	--	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	100	120	°C/W
Rthj-lead	Thermal Resistance Junction-lead Max	--	--	40	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		260	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	1.4	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	90	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate source Breakdown Voltage	I_{gs}= ± 1 mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1mA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.7 A		7.2	8	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D= 0.7 A		1		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		170 27 5		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 480V		30		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 300 V, I_D = 0.65 A, R_G= 4.7 Ω, V_{GS} = 10 V (Resistive Load see, Figure 22)		8 30 22 55		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 480V, I_D = 1.5 A, V_{GS} = 10V (see, Figure 24)		7.7 1.7 4	10	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				1.5 6	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 1.5 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1.3 A, di/dt = 100 A/µs V_{DD} = 25V, T_j = 25°C (see test circuit, Figure 23)		250 550 4.4		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1.3 A, di/dt = 100 A/µs V_{DD} = 25V, T_j = 150°C (see test circuit, Figure 23)		300 690 4.6		ns µC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Figure 3: .Safe Operating Area For TO-220

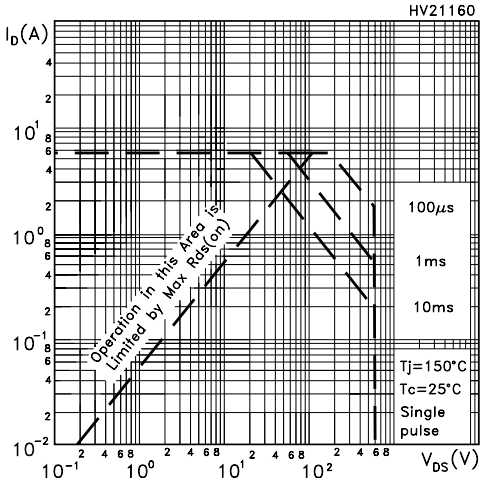


Figure 4: Safe Operating Area For IPAK

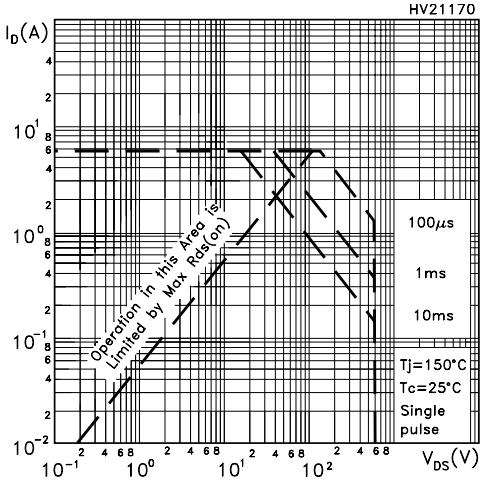


Figure 5: Safe Operating Area For TO-92

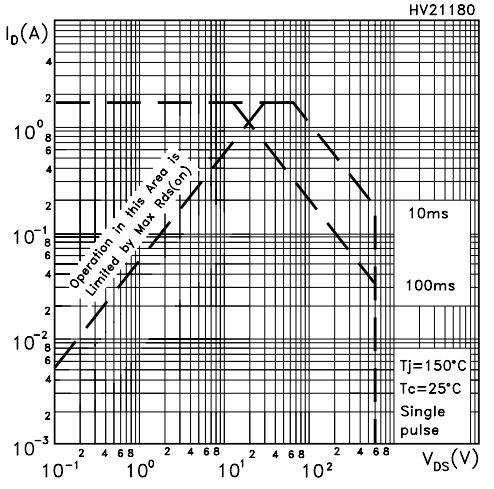


Figure 6: Thermal Impedance For TO-220

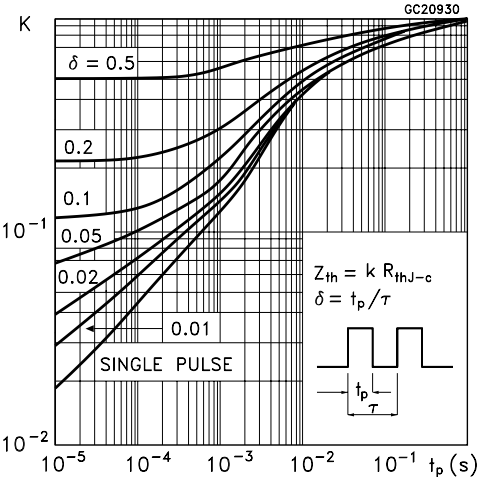


Figure 7: Thermal Impedance For IPAK

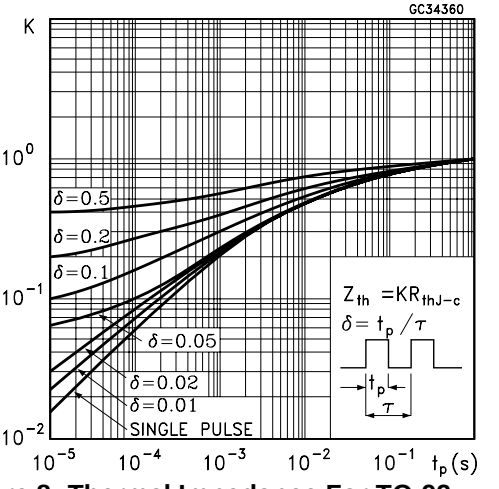


Figure 8: Thermal Impedance For TO-92