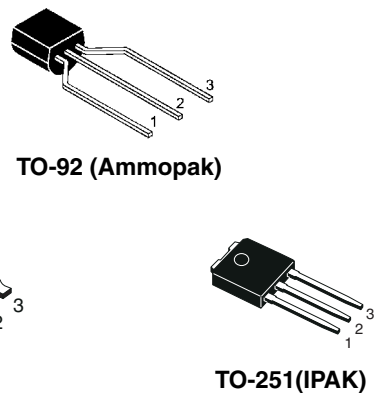
STD1LNK60Z-1
STQ1NK60ZR-AP - STN1NK60Z

N-channel 600V - 13Ω - 0.8A - TO-92 - TO-251 - SOT-223
Zener-Protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STD1LNK60Z-1	600V	<15Ω	0.8A	25W
STQ1NK60ZR-AP	600V	<15Ω	0.3A	3W
STN1NK60Z	600V	<15Ω	0.3A	3.3W

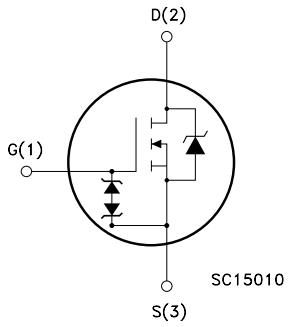
- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- ESD improved capability
- New high voltage benchmark



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram



Application

- Switching applications

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD1LNK60Z-1	D1LNK60Z	TO-251(IPAK)	Tube
STQ1NK60ZR-AP	1NK60ZR	TO-92	Ammopak
STN1NK60Z	1NK60Z	SOT-223	Tape & reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		IPAK	TO-92	SOT-223	
V_{DS}	Drain-source voltage (V_{GS} = 0)	600			V
V_{GS}	Gate-source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25°C	0.8	0.3	0.3	A
I_D	Drain current (continuous) at T_C=100°C	0.5	0.189		A
I_{DM}(1)	Drain current (pulsed)	3.2	1.2		A
P_{TOT}	Total dissipation at T_C = 25°C	25	3	3.3	W
	Derating factor	0.24	0.25	0.26	W/°C
$V_{ESD(G-D)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	800			V
dv/dt(2)	Peak diode recovery voltage slope	4.5			V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤0.3A, di/dt ≤200A/µs, V_{DD} =80%$V_{(BR)DSS}$

Table 3. Thermal resistance

Symbol	Parameter	Value			Unit
		IPAK	TO-92	SOT-223	
$R_{thj-case}$	Thermal resistance junction-case Max	5	--	--	°C/W
R_{thj-a}	Thermal resistance junction-ambient Max	100	120	37.87(1)	°C/W
$R_{thj-lead}$	Thermal resistance junction-lead Max	--	40	--	°C/W
T_l	Maximum lead temperature for soldering purpose	275	260		°C

1. When mounted on 1 inch² FR-4 board, 2 Oz Cu

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	0.8	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	60	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 0.4A		13	15	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 0.4A		0.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		94 17.6 2.8		pF pF pF
$C_{oss\ eq}$(2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 480V		11		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=480V, I_D = 0.8A V_{GS} =10V		4.9 1 2.7	6.9	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=300 V, I_D= 0.4A, R_G=4.7Ω, V_{GS}=10V		5.5 5 13 28		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				0.8	A
I_{SDM}(1)	Source-drain current (pulsed)				2.4	A
V_{SD}(2)	Forward on voltage	I_{SD}=0.8A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=0.8A, di/dt = 100A/µs, V_{DD}=20V, Tj=25°C		135 216 3.2		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=0.8A, di/dt = 100A/µs, V_{DD}=20V, Tj=150°C		140 224 3.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=±1mA (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for IPAK

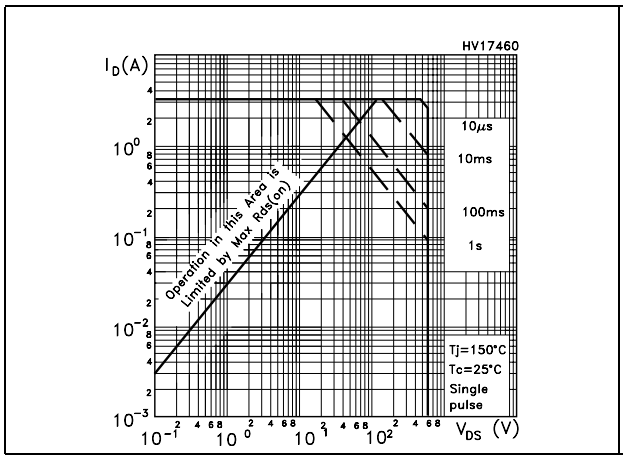


Figure 3. Thermal impedance for IPAK

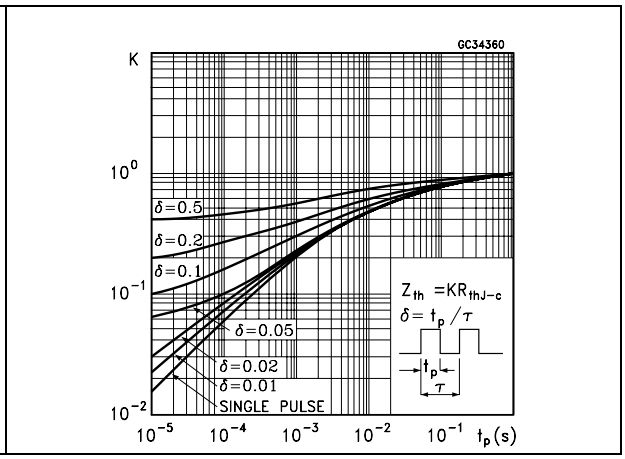


Figure 4. Safe operating area for TO-92

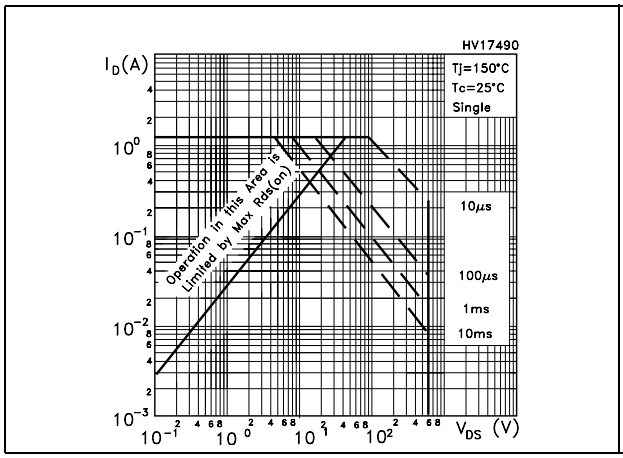


Figure 5. Thermal impedance for TO-92

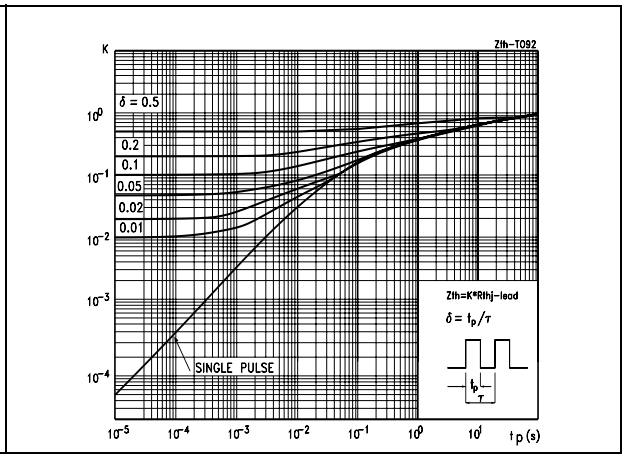


Figure 6. Safe operating area for SOT-223

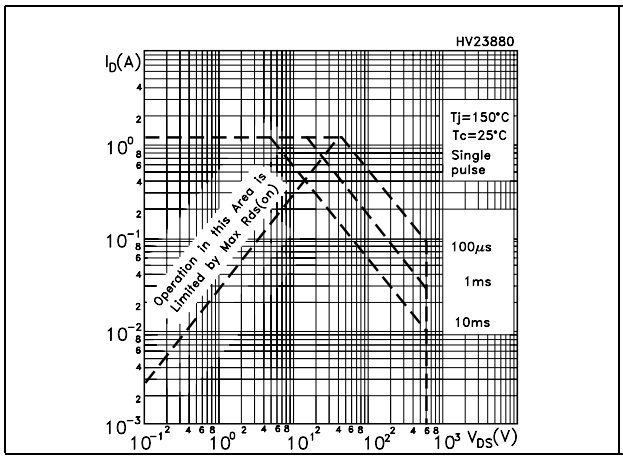


Figure 7. Thermal impedance for SOT-223