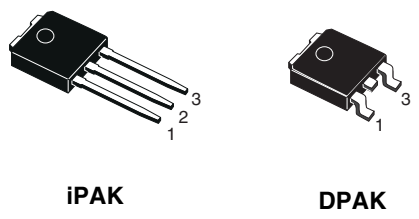
STD17NF03L
STD17NF03L-1

N-channel 30V - 0.038Ω - 17A - DPAK/IPAK
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STD17NF03L-1	30V	<0.05Ω	17A
STD17NF03L	30V	<0.05Ω	17A

- Exceptional dv/dt capability
- Low gate charge at 100°C
- Application oriented characterization
- 100% avalanche tested



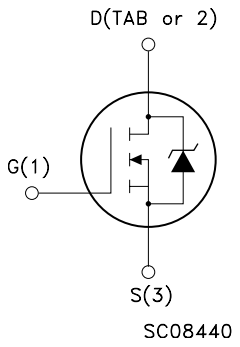
Description

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD17NF03L-1	D17NF03L@	IPAK	Tube
STD17NF03LT4	D17NF03L@	DPAK	Tape & reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source voltage	± 16	V
I_D	Drain current (continuous) at T_C = 25°C	17	A
I_D	Drain current (continuous) at T_C = 100°C	12	A
I_{DM}(1)	Drain current (pulsed)	68	A
P_{tot}	Total dissipation at T_C = 25°C	30	W
	Derating Factor	0.2	W/°C
dv/dt(2)	Peak diode recovery avalanche energy	7	V/ns
E_{AS} (3)	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 17A$, di/dt ≤300A/µs, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting T_j = 25 °C, I_D = 8.5A, V_{DD} = 15V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	5.0	°C/W
Rthj-amb	Thermal resistance junction-to ambient max	100	°C/W
T_J	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1	1.5	2.2	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 8.5A V_{GS} = 5V, I_D = 8.5A		0.038 0.045	0.05 0.06	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, , I_D =8.5A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		320 155 28		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 15V, I_D = 8.5A R_G = 4.7Ω V_{GS} = 5V		11 100 25 22		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 3024V, I_D = 17A, V_{GS} = 5V, R_G = 4.7Ω		4.8 2.25 1.7	6.5	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				22 88	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 17A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17A, di/dt = 100A/µs, V_{DD} = 15V, T_j = 150°C		28 18 1.3		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %