STD12NF06-1
STD12NF06

N-channel 60V - 0.08Ω - 12A - DPAK - IPAK
STripFET™ II Power MOSFET

General features

Type	V_{DSSS}	$R_{DS(on)}$	I_D
STD12NF06	60V	<0.1Ω	12A
STD12NF06-1	60V	<0.1Ω	12A

- Exceptional dv/dt capability
- Low gate charge

DPAK IPAK

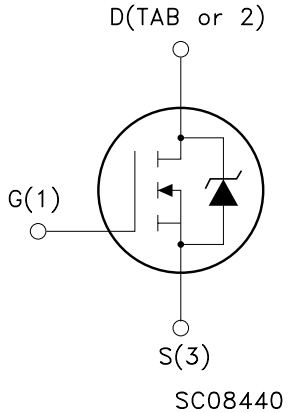
Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD12NF06T4	D12NF06	DPAK	Tape & reel
STD12NF06-1	D12NF06	IPAK	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	12	A
I_D	Drain current (continuous) at T_C=100°C	8.5	A
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25°C	30	W
	Derating factor	0.2	W/°C
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
E_{AS} (3)	Single pulse avalanche energy	140	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 12A$, di/dt $\leq 200A/\mu s$, $V_{DS} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
3. Starting T_J = 25 °C, I_D = 6A, V_{DD} = 30V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	5	°C/W
R_{thJA}	Thermal resistance junction-ambient Max	100	°C/W
T_l	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 25mA, V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 6A		0.08	0.1	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 6A		5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		315 70 30		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 48V, I_D = 12A V_{GS} = 10V		10 3.0 3.5	12	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 30V, I_D = 6A, R_G = 4.7Ω, V_{GS} = 10V		7 18 17 6		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				12	A
I_{SDM}	Source-drain current (pulsed)				48	A
V_{SD}(1)	Forward on voltage	I_{SD} = 12A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 12A, di/dt = 100A/µs, V_{DD} = 30V, T_J = 150°C		50 65 3.5		ns µC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

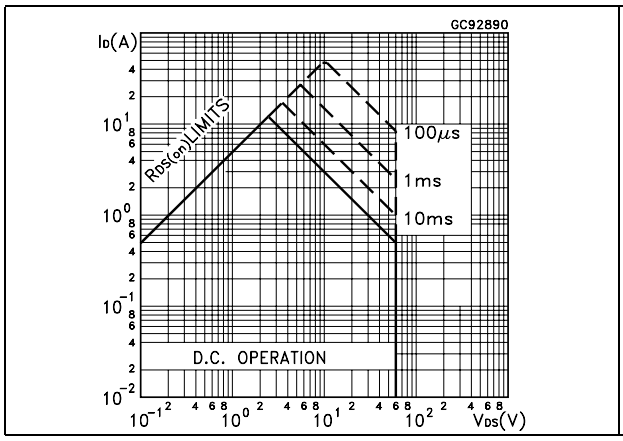


Figure 2. Thermal impedance

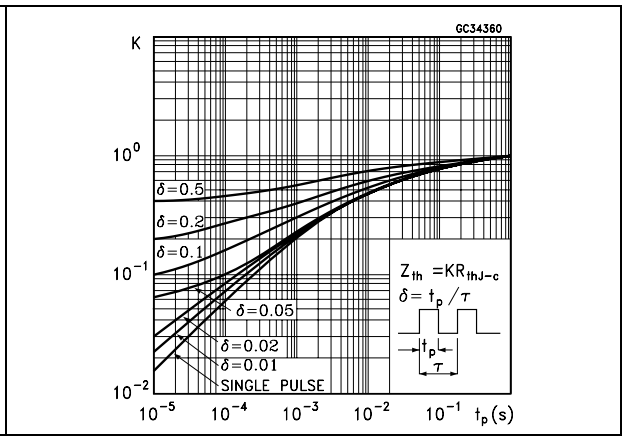


Figure 3. Output characteristics

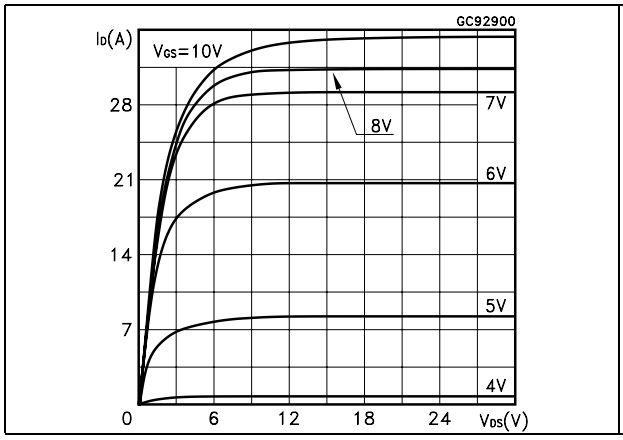


Figure 4. Transfer characteristics

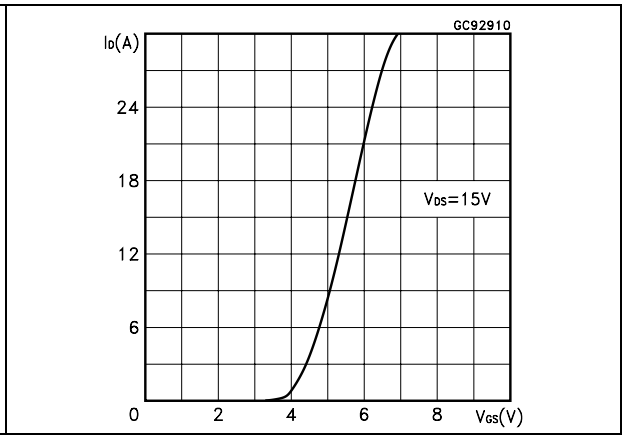


Figure 5. Transconductance

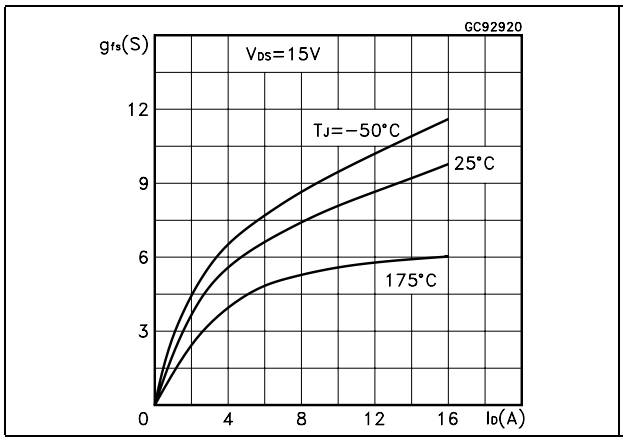


Figure 6. Static drain-source on resistance