1A, 55V, 0.750 Ohm,Voltage Clamping, Current Limited, N-Channel Power MOSFET

The RLP1N06CLE is an intelligent monolithic power circuit which incorporates a lateral bipolar transistor, resistors, zener diodes, and a PowerMOS transistor. The current limiting of this device allows it to be used safely in circuits where it is anticipated that a shorted load condition may be encountered. The drain to source voltage clamping offers precision control of the circuit voltage when switching inductive loads. Logic level gates allow this device to be fully biased on with only 5V from gate to source. Input protection is provided for ESD up to 2kV.

Formerly developmental type TA09880.

Ordering Information

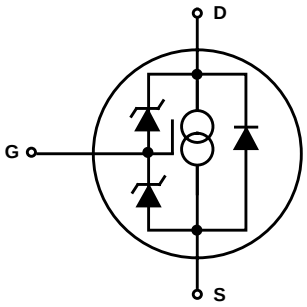
PART NUMBER	PACKAGE	BRAND
RLP1N06CLE	TO-220AB	L1N06CLE

NOTE: When ordering, use the entire part number.

Features

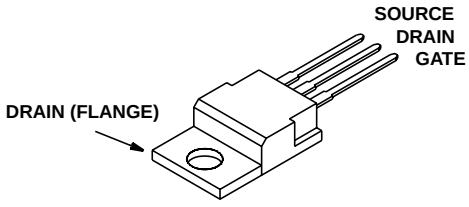
- 1A, 55V
- $r_{DS(ON)}$ = 0.750Ω
- I_{LIMIT} at 150^{O}C = 1.1A to 1.5A Maximum
- Built-in Voltage Clamp
- Built-in Current Limiting
- ESD Protected, 2kV Minimum
- Controlled Switching Limits EMI and RFI
- 175^{O}C Rated Junction Temperature
- Logic Level Gate
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RLP1N06CLE	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ, Note 1)	V_{DGR}	55	V
Electrostatic Voltage at $T_C = 25^oC$	ESD	2	kV
Continuous Drain Current	I_D	Self Limited	
Gate to Source Voltage (Reverse Voltage Gate Bias Not Allowed)	V_{GS}	5.5	V
Maximum Power Dissipation	P_D	36	W
Power Dissipation Derating		0.24	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 20mA, V_{GS} = 0V (Figure 7)		55	-	70	V
Gate to Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 8)		1	-	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 45V, V_{GS} = 0V	TC = 25^oC	-	-	5	μA
			TC = 150^oC	-	-	20	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 5V	TC = 25^oC	-	-	5	μA
			T_C = 150^oC	-	-	20	μA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1A, V_{GS} = 5V (Figure 6)	TC = 25^oC	-	-	0.750	Ω
			T_C = 150^oC	-	-	1.500	Ω
Limiting Current	$I_{DS(LIM)}$	V_{DS} = 15V, V_{GS} = 5V (Figure 2)	TC = 25^oC	1.8	-	3	A
			T_C = 150^oC	0.9	-	1.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30V, I_D = 1A, V_{GS} = 5V, R_{GS} = 25Ω R_L = 30Ω		-	-	6.5	μs
Turn-On Delay Time	$t_{d(ON)}$			-	-	1.5	μs
Rise Time	t_r			1	-	5	μs
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	7.5	μs
Fall Time	t_f			1	-	5	μs
Turn-Off Time	$t_{(OFF)}$			-	-	12.5	μs
Thermal Resistance Junction to Case	$R_{θJC}$			-	-	4.17	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{θJA}$	TO-220AA		-	-	62	$^oC/W$
Electrostatic Voltage	ESD	Human Model (100pF, 1.5kΩ) MIL-STD-883B (Category B2)		2000	-	-	V

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 1A	-	-	1	ms

NOTES:

2. Pulsed: pulse duration = 80μs maximum, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

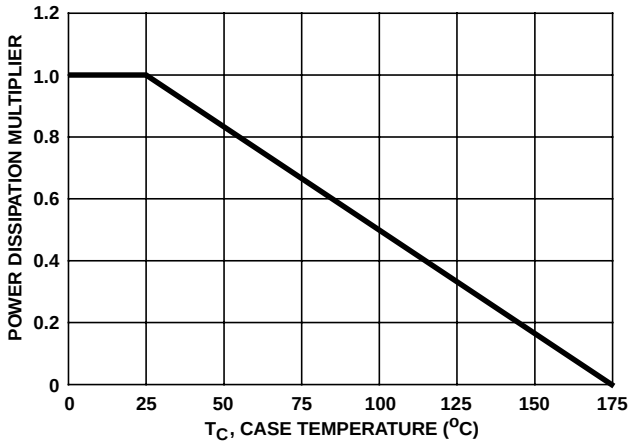


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

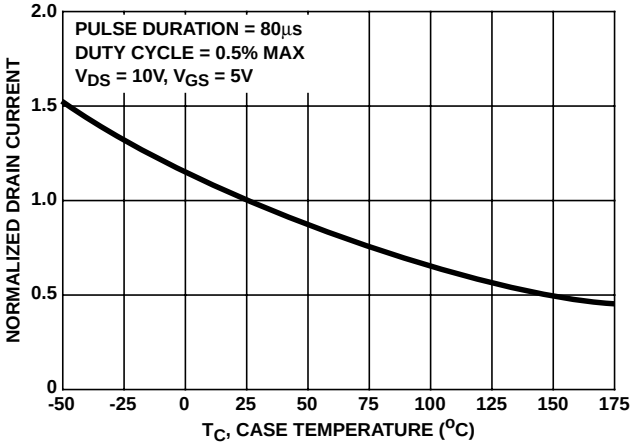


FIGURE 2. NORMALIZED CURRENT LIMIT vs CASE TEMPERATURE

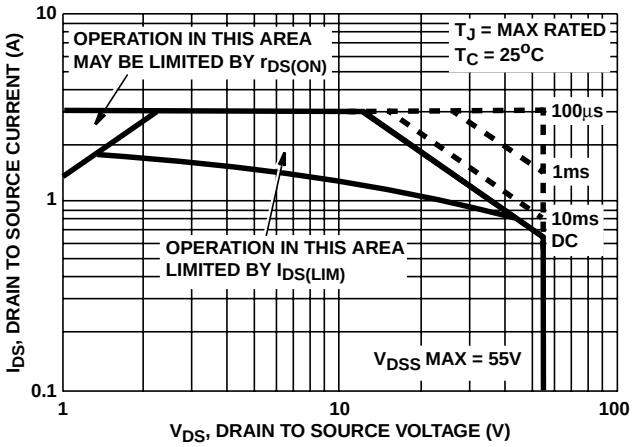


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

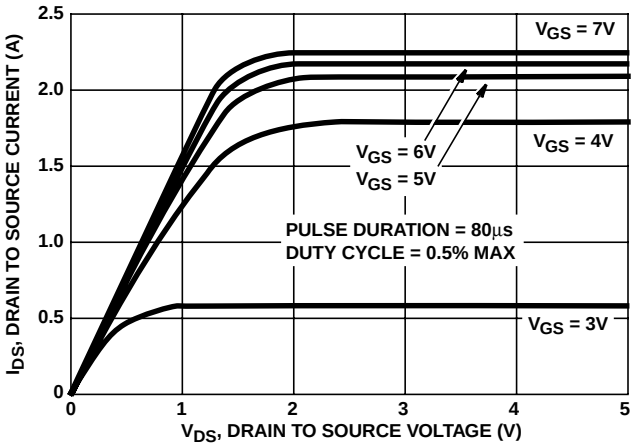


FIGURE 4. SATURATION CHARACTERISTICS

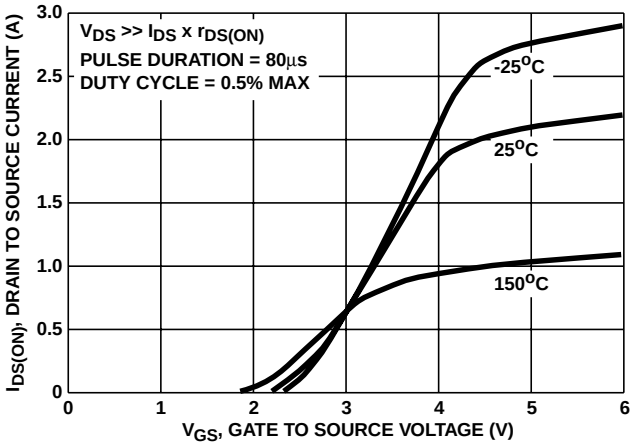


FIGURE 5. TRANSFER CHARACTERISTICS

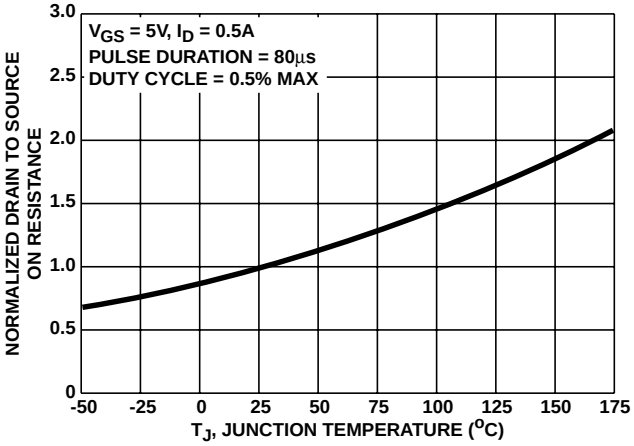


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE