40A, 100V, 0.040 Ohm, N-Channel Power MOSFETs

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA9846

Ordering Information

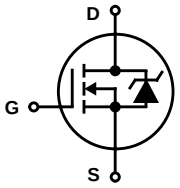
PART NUMBER	PACKAGE	BRAND
RFG40N10	TO-247	RFG40N10
RFP40N10	TO-220AB	RFP40N10
RF1S40N10SM	TO-263AB	F1S40N10

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S40N10SM9A.

Features

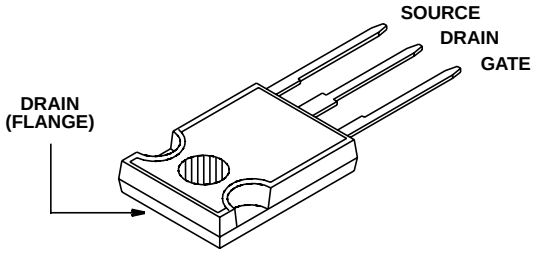
- 40A, 100V
- $r_{DS(ON)} = 0.040\Omega$
- UIS Rating Curve
- SOA is Power Dissipation Limited
- $175^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

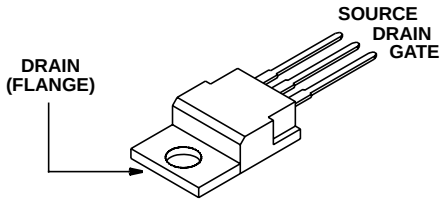


Packaging

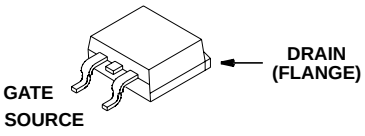
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG40N10, RFP40N10, RF1S40N10SM	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DSS}	100	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	40	A
Pulsed Drain Current (Note 2)	I_{DM}	100	A
Pulsed Avalanche Rating	E_{AS}	Figures 4, 12, 13	
Power Dissipation	P_D	160	W
Derate Above 25^oC		1.07	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	^oC
Package Body for 10s, see Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. $T_J = 25^oC$ to 150^oC.
2. Repetitive Rating: pulse width limited by maximum junction temperature.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 9)		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 8)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V	$T_C = 25^oC$	-	-	1	μA
			$T_C = 150^oC$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 40A, V_{GS} = 10V (Figure 7)		-	-	0.040	Ω
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 20A, R_L = 2.5Ω, V_{GS} = 10V, R_{GS} = 4.2 Ω (Figure 11)		-	-	80	ns
Turn-On Delay Time	$t_{d(ON)}$			-	17	-	ns
Rise Time	t_r			-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	42	-	ns
Fall Time	t_f			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 80V, I_D = 40A, R_L = 2.0Ω (Figures 11)	-	-	300	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	-	150	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	-	7.5	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.94	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220AB and TO-263AB		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 40A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 40A, dI_{SD}/dt = 100A/μs	-	-	200	ns

Typical Performance Curves Unless Otherwise Specified

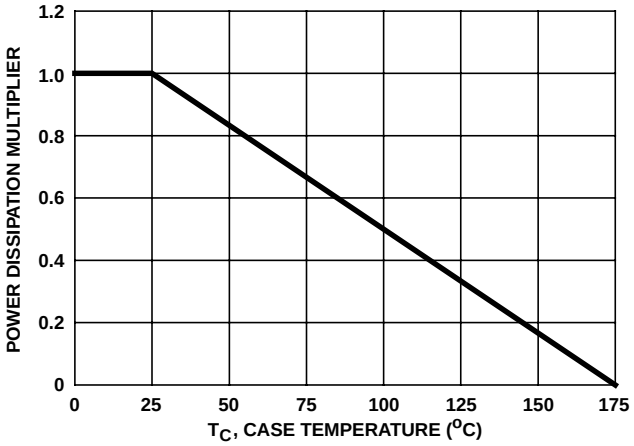


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

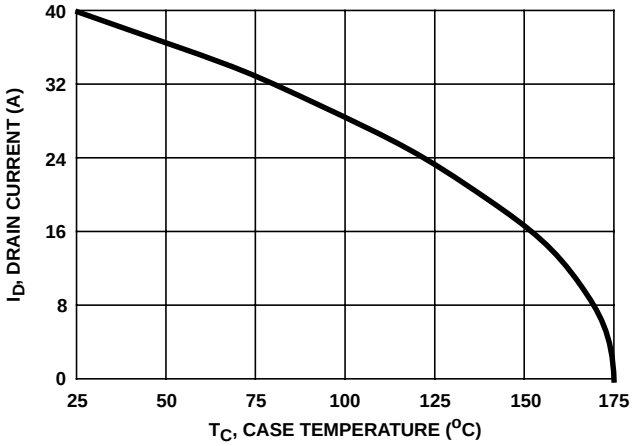


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

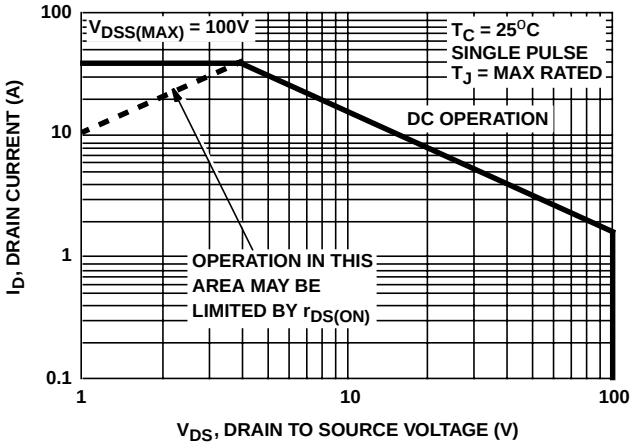
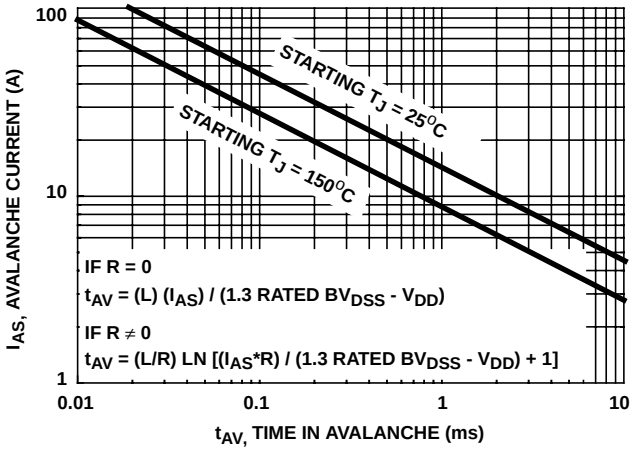


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil application notes AN9321 and AN9322.

FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

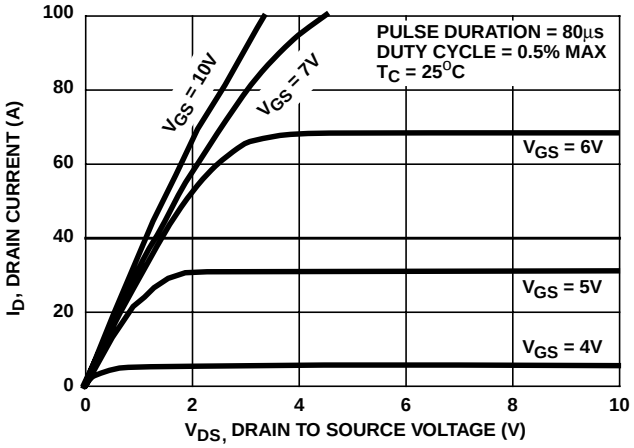


FIGURE 5. SATURATION CHARACTERISTICS

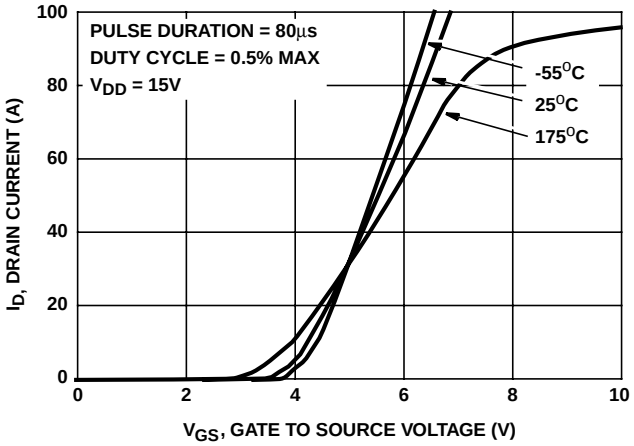


FIGURE 6. TRANSFER CHARACTERISTICS