

Features

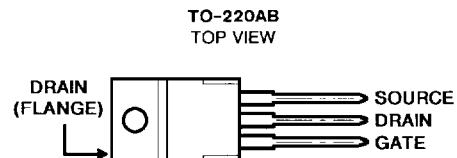
- 17A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The RFP17N06L is an N-Channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V – 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

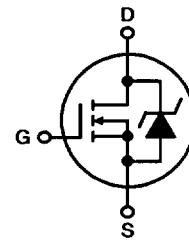
The RFP17N06L is supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ C$) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	17	A
Pulsed Drain Current	I_{DM}	50	A
Gate-Source Voltage	V_{GS}	± 10	V
Maximum Power Dissipation			
$T_C = +25^\circ C$	P_D	60	W
Above $T_C = +25^\circ C$, Derate Linearly		0.48	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Specifications RFP17N06L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		MIN.	MAX.	
Drain-Source Breakdown Voltage BV_{DSS}	$I_D = 1.0 \text{ mA}, V_{GS} = 0 \text{ V}$	60	—	V
Gate Threshold Voltage $V_{GS(\text{th})}$	$V_{GS} = V_{DS}, I_D = 1.0 \text{ mA}$	1	2	
Zero Gate Voltage Drain Current I_{DSS}	$V_{DS} = 48\text{V}, V_{GS} = 0 \text{ V}$ $T_C = 150^\circ\text{C}$	—	1 50	μA
Gate-Source Leakage Current I_{GSS}	$V_{GS} = \pm 10 \text{ V}$	—	100	nA
On Resistance $R_{DS(\text{on})}$	$I_D = 8.5 \text{ A}, V_{GS} = 4.0 \text{ V}$	—	0.150	Ω
	$I_D = 8.5 \text{ A}, V_{GS} = 5.0 \text{ V}$	—	0.100	
	$I_D = 17.0 \text{ A}, V_{GS} = 5.0 \text{ V}$	—	0.130	
Forward Transconductance g_{FS}	$I_D = 8.5 \text{ A}, V_{DS} = 5.0 \text{ V}$	6.0	—	S
Turn-On Delay Time $T_{d(\text{on})}$	$V_{DD} = 30 \text{ V}, I_D = 8.5 \text{ A}$	—	40	ns
Rise Time T_R	$R_{GEN} = 12.5 \text{ ohms}$	—	150	
Turn-Off Delay Time $T_{d(\text{off})}$	$R_{GS} = 12.5 \text{ ohms}$	—	240	
Fall Time T_F	$V_{GS} = +5 \text{ V}$	—	110	
Total Gate Charge $Q_g(\text{total})$	$I_D = 8.5 \text{ A}, V_{DD} = 30 \text{ V}$ $V_{GS} = 10 \text{ V}, R_L = 3.5 \text{ ohms}$	—	45	nC
Gate Charge at 5 volts $Q_g(5)$	$V_{GS} = 5 \text{ V}$	—	25	
Threshold Gate Charge $Q_g(\text{th})$	$V_{GS} = 1 \text{ V}$	—	2.0	
Thermal Resistance Junction to Case $R_{\theta JC}$		—	2.083	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient $R_{\theta JA}$		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		MIN.	MAX.	
Forward Voltage V_{SD}	$I_{SD} = 17 \text{ A}$	—	1.2	V
Reverse Recovery Time t_r	$I_F = 17 \text{ A}, dI_F/dt = 100 \text{ A}/\mu\text{s}$	115 (typ)		ns

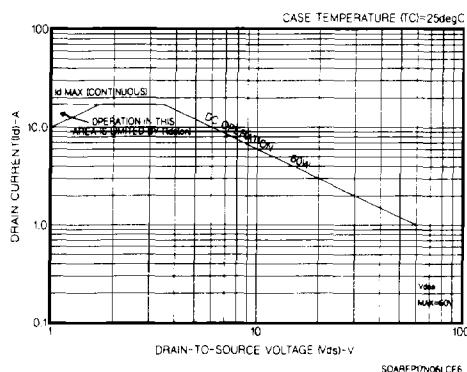


Fig. 1 - Maximum safe operating areas for all types.