

**10A, 30V, 0.200 Ohm, Logic Level,  
P-Channel Power MOSFET**

These products are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49205.

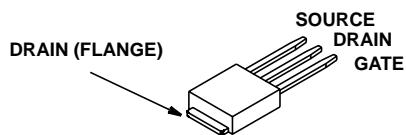
**Ordering Information**

PART NUMBER	PACKAGE	BRAND
RFD10P03L	TO-251AA	10P03L
RFD10P03LSM	TO-252AA	10P03L
RFP10P03L	TO-220AB	F10P03L

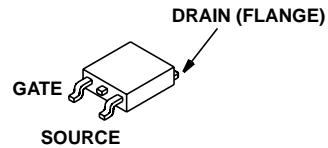
NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD10P03LSM9A..

**Packaging**

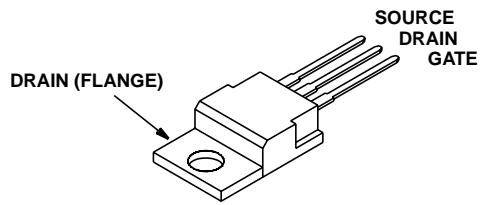
JEDEC TO-251AA



JEDEC TO-252AA



JEDEC TO-220AB



# RFD10P03L, RFD10P03LSM, RFP10P03L

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ Unless Otherwise Specified

		RFD10P03L, RFD10P03LSM, RFP10P03L	UNITS
Drain to Source Voltage.....	$V_{DSS}$	-30	V
Drain to Gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ ).....	$V_{DGR}$	-30	V
Gate to Source Voltage .....	$V_{GS}$	$\pm 10$	V
Drain Current			
RMS Continuous .....	$I_D$	10	A
Pulsed Drain Current .....	$I_{DM}$	See Figure 5	
Single Pulse Avalanche Rating .....	$E_{AS}$	Refer to UIS Curve	
Power Dissipation .....	$P_D$	65	W
Derate Above $25^\circ\text{C}$ .....		0.43	$W/\text{ }^\circ\text{C}$
Operating and Storage Temperature .....	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Maximum Lead Temperature for Soldering .....	$T_L$	300	$^\circ\text{C}$
(0.063in (1.6mm) from case for 10s)			

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	-30	-	-	V
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 12)	-1	-	-2	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{V}, T_C = 25^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	-50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 1)	$r_{DS(\text{ON})}$	$I_D = 10\text{A}, V_{GS} = -5\text{V}$ (Figures 9, 10)	-	-	0.200	$\Omega$
		$I_D = 10\text{A}, V_{GS} = -4.5\text{V}$ (Figures 9, 10)			0.220	$\Omega$
Turn-On Time	$t_{\text{ON}}$	$V_{DD} = 15\text{V}, I_D \geq 10\text{A}, R_L = 1.5\Omega, R_{GS} = 5\Omega, V_{GS} = -5\text{V}$ (Figure 13)	-	-	100	ns
Turn-On Delay Time	$t_{d(\text{ON})}$		-	15	-	ns
Rise Time	$t_r$		-	50	-	ns
Turn-Off Delay Time	$t_{d(\text{OFF})}$		-	35	-	ns
Fall Time	$t_f$		-	20	-	ns
Turn-Off Time	$t_{\text{OFF}}$		-	-	80	ns
Total Gate Charge	$Q_{g(\text{TOT})}$		-	25	30	nC
Gate Charge at $-5\text{V}$	$Q_{g(-5)}$	$V_{GS} = 0$ to $-5\text{V}$	-	13	16	nC
Threshold Gate Charge	$Q_{g(\text{TH})}$	$V_{GS} = 0$ to $-1\text{V}$	-	1.2	1.5	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 15)	-	1035	-	pF
Output Capacitance	$C_{OSS}$		-	340	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	35	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	-	2.30	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	RFD10P03L, RFD10P03LSM	-	-	100	$^\circ\text{C}/\text{W}$
		RFP10P03L			80	$^\circ\text{C}/\text{W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Forward Voltage	$V_{SD}$	$I_{SD} = -10\text{A}$	-	-	-1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = -10\text{A}, dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	75	ns

### NOTE:

- Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

**Typical Performance Curves** Unless Otherwise Specified

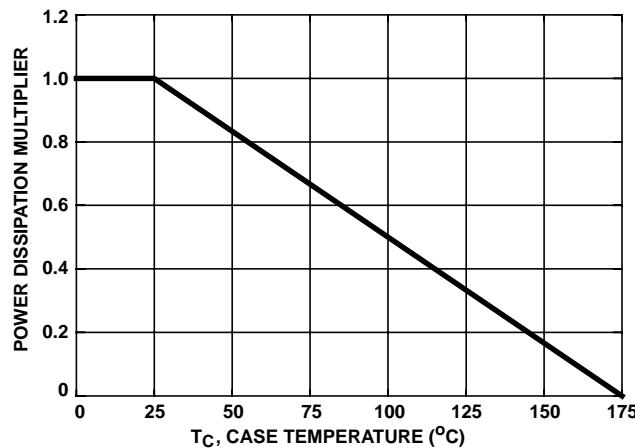


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

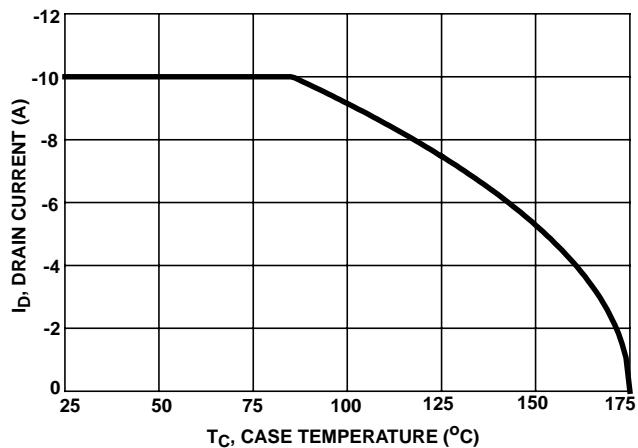


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

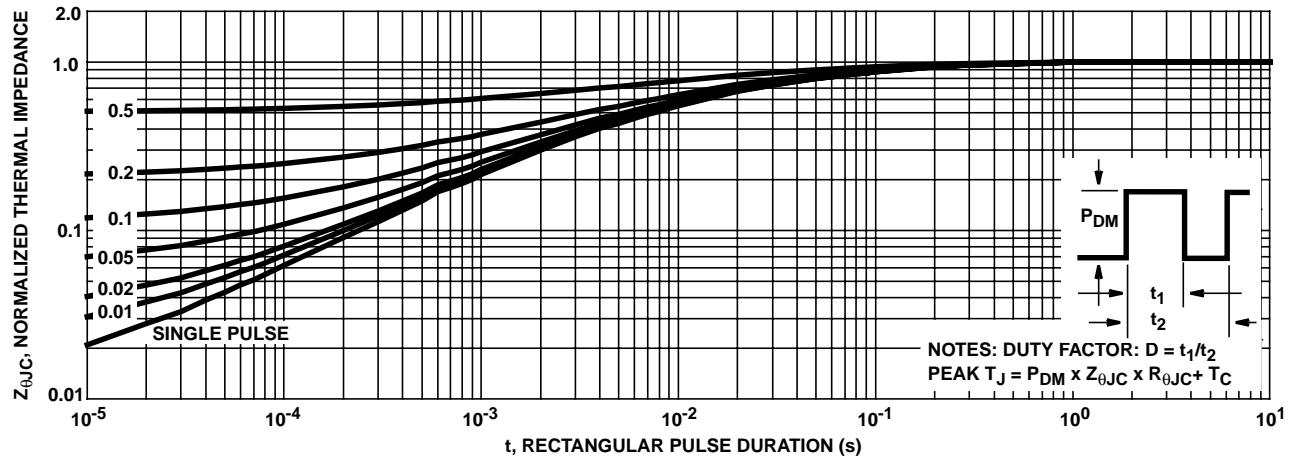


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

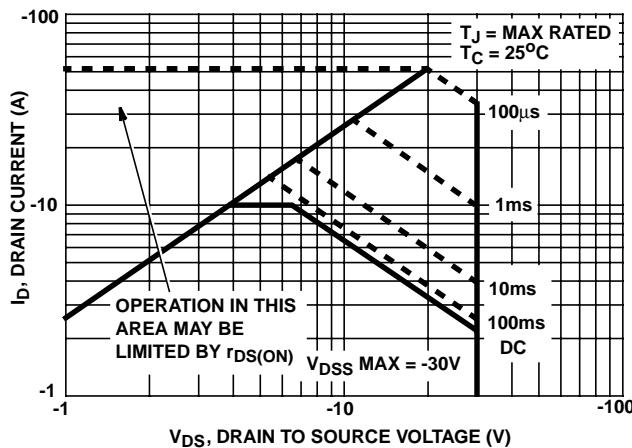


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

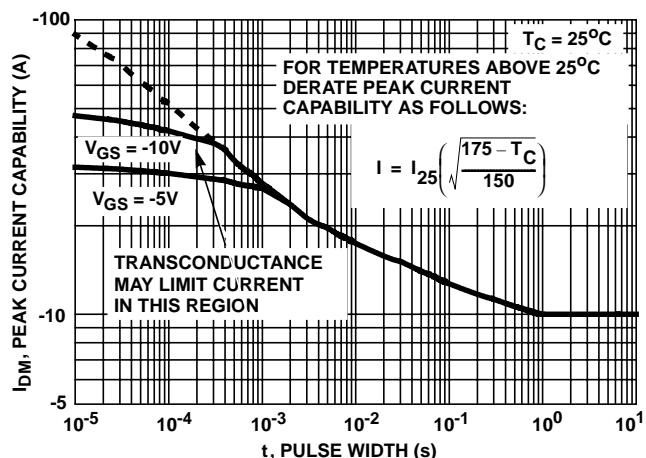


FIGURE 5. PEAK CURRENT CAPABILITY