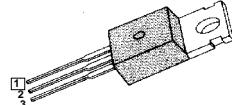


FEATURES

- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ Lower Leakage Current: 10 μ A (Max.) @ V_{DS} = 100V
- ◆ Lower R_{DS(ON)}: 0.046 Ω (Typ.)

BV_{DSS} = 100 V
R_{DS(on)} = 0.058 Ω
I_D = 28 A

TO-220



1.Gate 2.Drain 3.Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V _{DSS}	Drain-to-Source Voltage	100	V
I _D	Continuous Drain Current (T _C =25°C)	28	A
	Continuous Drain Current (T _C =100°C)	19.8	
I _{DM}	Drain Current-Pulsed (1)	98	A
V _{GS}	Gate-to-Source Voltage	\pm 20	V
E _{AS}	Single Pulsed Avalanche Energy (2)	522	mJ
I _{AR}	Avalanche Current (1)	28	A
E _{AR}	Repetitive Avalanche Energy (1)	12.1	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	6.5	V/ns
P _D	Total Power Dissipation (T _C =25°C)	121	W
	Linear Derating Factor	0.81	W/ $^{\circ}$ C
T _J , T _{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	$^{\circ}$ C
T _L	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	--	1.24	$^{\circ}$ C/W
R _{θCS}	Case-to-Sink	0.5	--	
R _{θJA}	Junction-to-Ambient	--	62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$
$\Delta \text{BV}/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.1	--	V/ $^\circ\text{C}$	$I_D=250\mu\text{A}$ See Fig 7
$V_{\text{GS(th)}}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{\text{DS}}=5\text{V}, I_D=250\mu\text{A}$
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	$V_{\text{GS}}=20\text{V}$
	Gate-Source Leakage , Reverse	--	--	-100		$V_{\text{GS}}=-20\text{V}$
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	$V_{\text{DS}}=100\text{V}$
		--	--	100		$V_{\text{DS}}=80\text{V}, T_C=150^\circ\text{C}$
$R_{\text{DS(on)}}$	Static Drain-Source On-State Resistance	--	--	0.058	Ω	$V_{\text{GS}}=5\text{V}, I_D=14\text{A}$ (4)
g_{fs}	Forward Transconductance	--	22	--	S	$V_{\text{DS}}=40\text{V}, I_D=14\text{A}$ (4)
C_{iss}	Input Capacitance	--	1215	1580	pF	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=25\text{V}, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	310	390		
C_{rss}	Reverse Transfer Capacitance	--	145	180		
$t_{\text{d(on)}}$	Turn-On Delay Time	--	7	25	ns	$V_{\text{DD}}=50\text{V}, I_D=28\text{A}, R_G=4.6\Omega$ See Fig 13 (4) (5)
t_r	Rise Time	--	12	35		
$t_{\text{d(off)}}$	Turn-Off Delay Time	--	38	85		
t_f	Fall Time	--	24	60		
Q_g	Total Gate Charge	--	38.4	54	nC	$V_{\text{DS}}=80\text{V}, V_{\text{GS}}=5\text{V}, I_D=28\text{A}$ See Fig 6 & Fig 12 (4) (5)
Q_{gs}	Gate-Source Charge	--	6.2	--		
Q_{gd}	Gate-Drain (. Miller.) Charge	--	23.3	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_s	Continuous Source Current	--	--	28	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current (1)	--	--	98		
V_{SD}	Diode Forward Voltage (4)	--	--	1.5	V	$T_J=25^\circ\text{C}, I_s=28\text{A}, V_{\text{GS}}=0\text{V}$
t_{rr}	Reverse Recovery Time	--	132	--	ns	$T_J=25^\circ\text{C}, I_F=28\text{A}$
Q_{rr}	Reverse Recovery Charge	--	0.63	--	μC	$di_F/dt=100\text{A}/\mu\text{s}$ (4)

Notes:

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2) $L=1\text{mH}, I_{AS}=28\text{A}, V_{DD}=25\text{V}, R_G=27\Omega$, Starting $T_J=25^\circ\text{C}$
- (3) $I_{SD} \leq 28\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq \text{BV}_{\text{DSS}}$, Starting $T_J=25^\circ\text{C}$
- (4) Pulse Test: Pulse Width = $250\mu\text{s}$, Duty Cycle $\leq 2\%$
- (5) Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

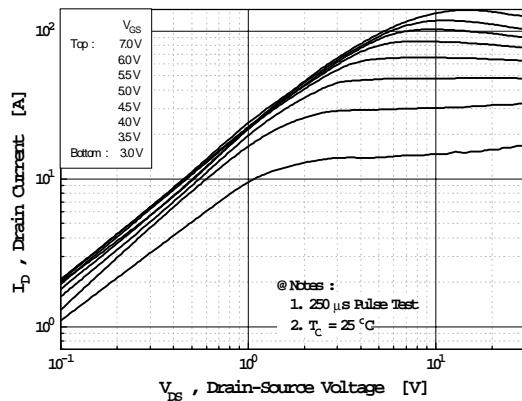


Fig 2. Transfer Characteristics

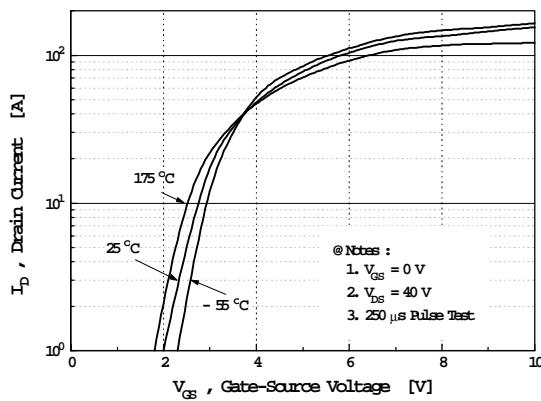


Fig 3. On-Resistance vs. Drain Current

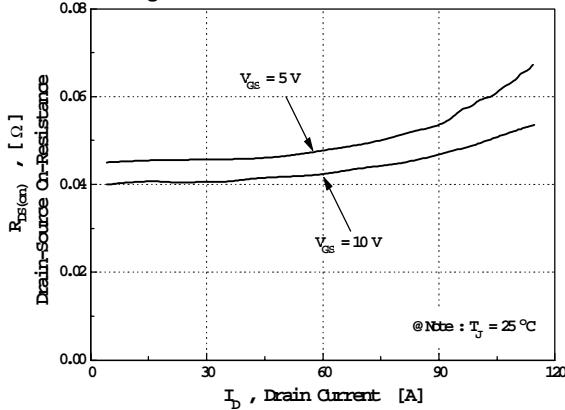


Fig 4. Source-Drain Diode Forward Voltage

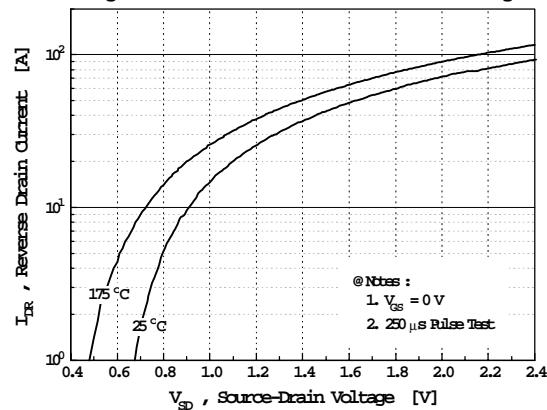


Fig 5. Capacitance vs. Drain-Source Voltage

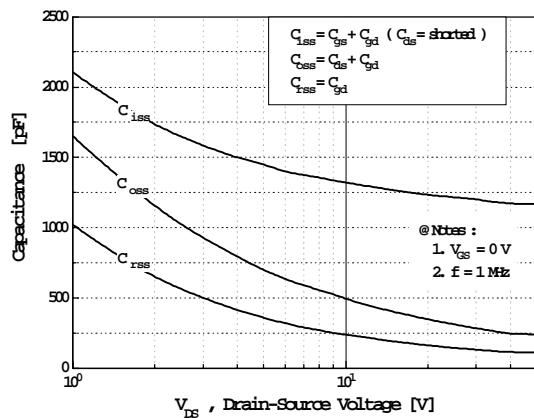


Fig 6. Gate Charge vs. Gate-Source Voltage

