75A, 30V, 0.009 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76137.

Ordering Information

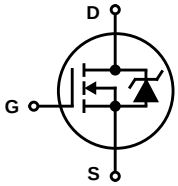
PART NUMBER	PACKAGE	BRAND
HUF76137P3	TO-220AB	76137P
HUF76137S3S	TO-263AB	76137S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76137S3ST.

Features

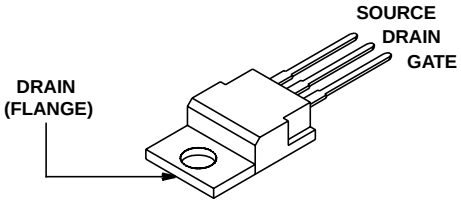
- Logic Level Gate Drive
- 75A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.009\Omega$
- Temperature Compensating PSPICE™ Model
- Temperature Compensating SABER Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

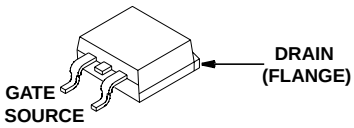


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous ($T_C = 25^oC$, V_{GS} = 10V) (Figure 2)	I_D	75	A
Continuous ($T_C = 100^oC$, V_{GS} = 5V)	I_D	55	A
Continuous ($T_C = 100^oC$, V_{GS} = 4.5V) (Figure 2)	I_D	52	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18	
Power Dissipation	P_D	145	W
Derate Above 25^oC		1.16	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-40 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 25V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figures 9, 10)	-	0.0075	0.009	Ω
		I_D = 55A, V_{GS} = 5V (Figure 9)	-	0.010	0.0125	Ω
		I_D = 52A, V_{GS} = 4.5V (Figure 9)	-	0.011	0.014	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	0.86	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 and TO-263	-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)						
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 52A, R_L = 0.289Ω, V_{GS} = 4.5V, R_{GS} = 5.1Ω (Figures 15, 21, 22)	-	-	420	ns
Turn-On Delay Time	$t_{d(ON)}$		-	20	-	ns
Rise Time	t_r		-	260	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	28	-	ns
Fall Time	t_f		-	38	-	ns
Turn-Off Time	t_{OFF}		-	-	100	ns

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 75A, R_L = 0.20Ω, V_{GS} = 10V, R_{GS} = 5.6Ω (Figures 16, 21, 22)		-	-	225	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	140	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	45	-	ns
Fall Time	t_f			-	35	-	ns
Turn-Off Time	t_{OFF}			-	-	120	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 15V, $I_D \cong$ 55A, R_L = 0.273Ω $I_{g(REF)}$ = 1.0mA (Figures 14, 19, 20)	-	55	72	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	31	40	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	2.2	2.9	nC
Gate to Source Gate Charge	Q_{gs}			-	6.00	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	15.50		nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	2100	-	pF
Output Capacitance	C_{OSS}			-	1050	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	225	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 55A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 55A, dI_{SD}/dt = 100A/µs	-	-	77	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 55A, dI_{SD}/dt = 100A/µs	-	-	143	nC

Typical Performance Curves

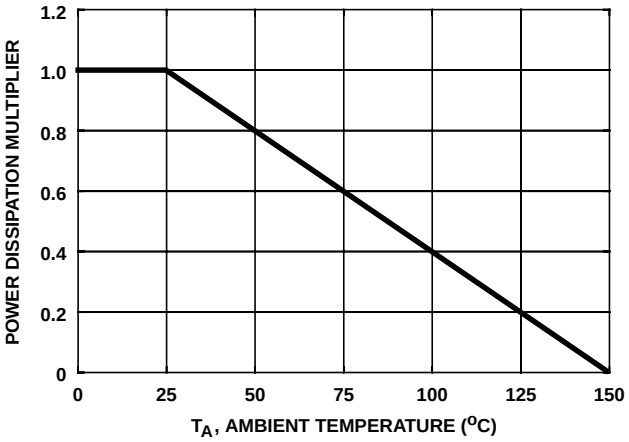


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

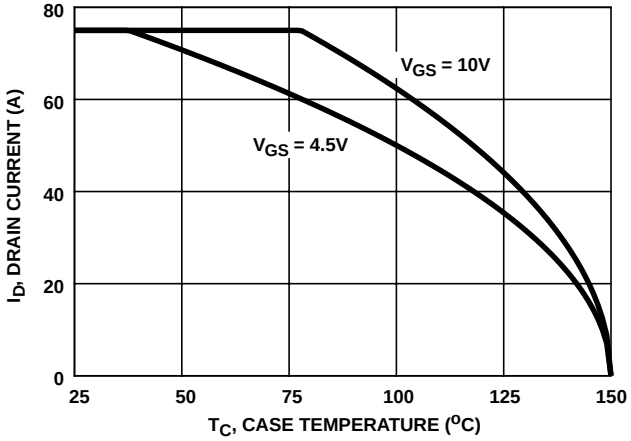


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE