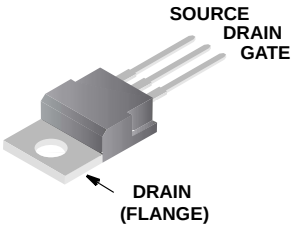
[redacted]

N-Channel UltraFET Power MOSFET
100 V, 75 A, 14 mΩ

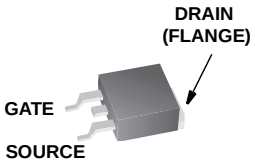
Packaging

JEDEC TO-220AB



HUF75645P3

JEDEC TO-263AB

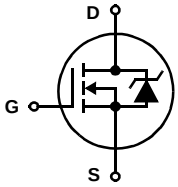


HUF75645S3ST

Features

- Ultra Low On-Resistance
  - $r_{DS(ON)}$ = 0.014Ω, V_{GS} = 10V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and Saber Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Symbol



Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75645P3	TO-220AB	75645P
HUF75645S3ST	TO-263AB	75645S

Absolute Maximum Ratings

T_C = 25°C, Unless Otherwise Specified

		HUF75645P3, HUF75645S3ST	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (T_C= 25°C, V_{GS} = 10V) (Figure 2)	I_D	75	A
Continuous (T_C= 100°C, V_{GS} = 10V) (Figure 2)	I_D	65	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 14, 15	
Power Dissipation	P_D	310	W
Derate Above 25°C		2.07	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	°C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	°C
Package Body for 10s, See Techbrief TB334	T_{pkg}	260	°C

NOTES:

1. T_J = 25°C to 150°C.

CAUTION: *Stresses above those listed in "Absol24ute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 11)	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 95V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 90V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA (Figure 10)	2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figure 9)	-	0.0115	0.014	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220 and TO-263	-	-	0.48	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 10V)						
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 75A V_{GS} = 10V, R_{GS} = 2.5Ω (Figures 18, 19)	-	-	197	ns
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns
Rise Time	t_r		-	117	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	41	-	ns
Fall Time	t_f		-	97	-	ns
Turn-Off Time	t_{OFF}		-	-	207	ns
GATE CHARGE SPECIFICATIONS						
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V; V_{DD} = 50V, I_D = 75A, $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	198	238	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V	-	106	127	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V	-	6.8	8.2	nC
Gate to Source Gate Charge	Q_{gs}		-	14	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	41	-	nC
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	3790	-	pF
Output Capacitance	C_{OSS}		-	810	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	230	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.25	V
		I_{SD} = 35A	-	-	1.00	V
Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	145	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	360	nC

Typical Performance Curves

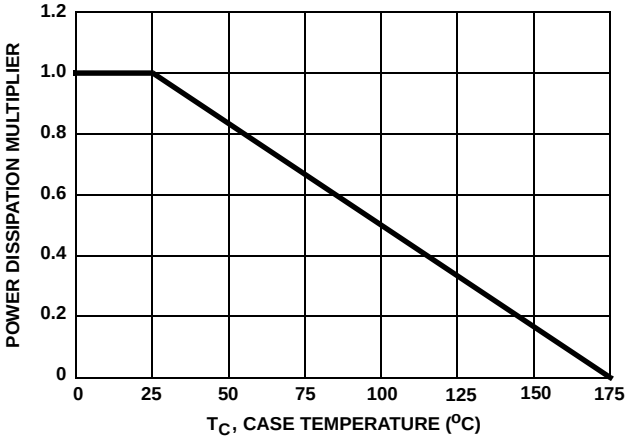


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

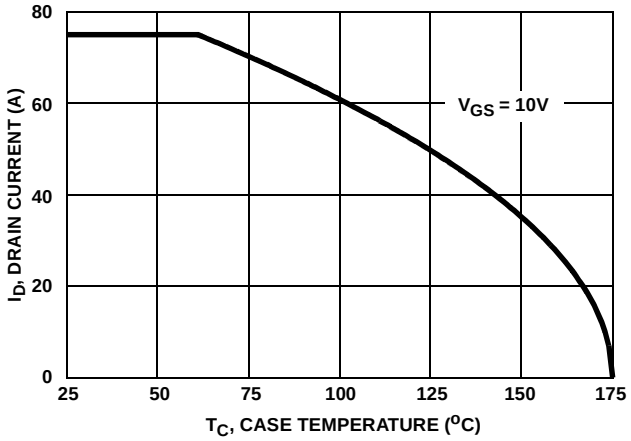


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

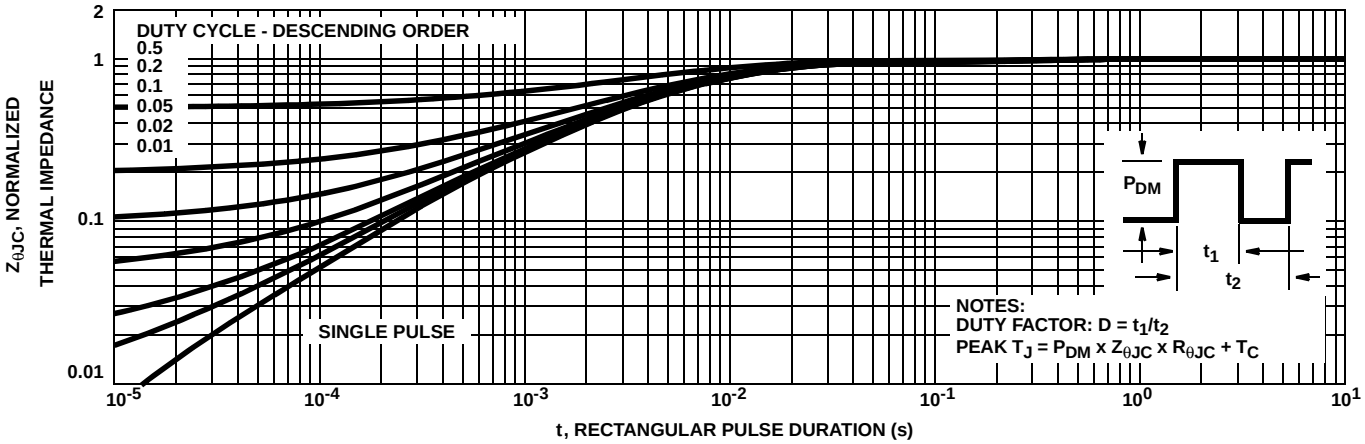


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

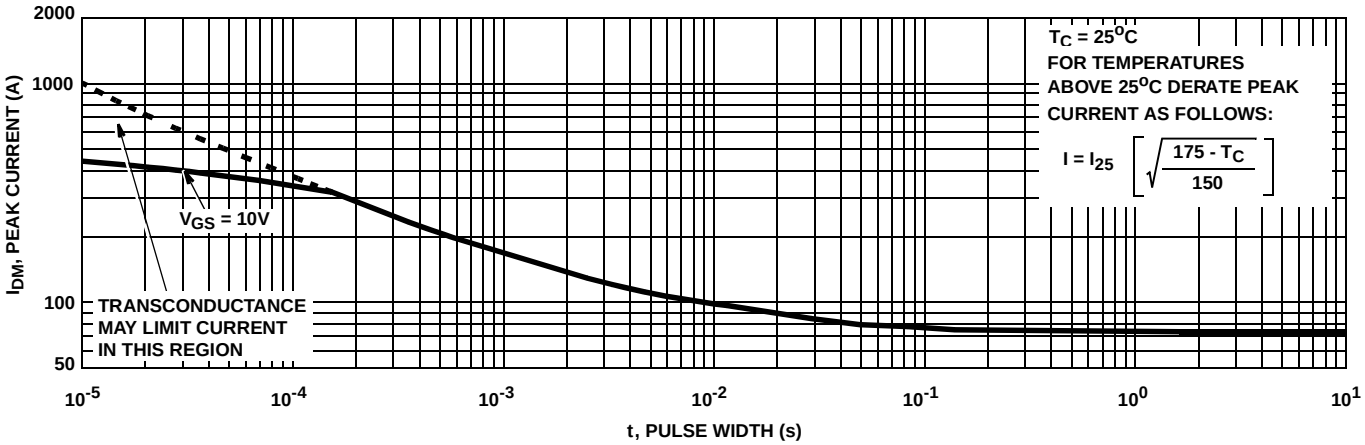


FIGURE 4. PEAK CURRENT CAPABILITY