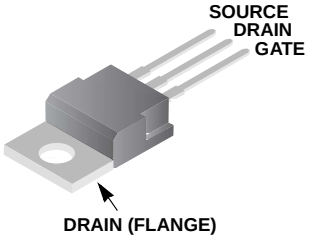
[redacted]

75A, 80V, 0.014 Ohm, N-Channel, UltraFET Power MOSFETs

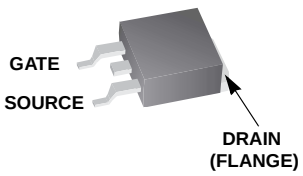
Packaging

JEDEC TO-220AB



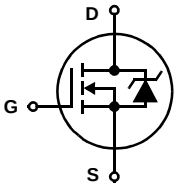
HUF75542P3

JEDEC TO-263AB



HUF75542S3S

Symbol



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.014\Omega$, $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75542P3	TO-220AB	75542P
HUF75542S3S	TO-263AB	75542S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF75542S3ST.

Absolute Maximum Ratings

$T_C = 25^oC$, Unless Otherwise Specified

		HUF75542P3, HUF75542S3S	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	80	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	80	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous ($T_C = 25^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	75	A
Continuous ($T_C = 100^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	58	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 14, 15	
Power Dissipation	P_D	230	W
Derate Above 25^oC		1.54	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief TB334	T_{pkg}	260	^oC

NOTE:

1. $T_J = 25^oC$ to 150^oC.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 11)	80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 75V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 70V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA (Figure 10)	2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figure 9)	-	0.012	0.014	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220 and TO-263	-	-	0.65	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 10V)						
Turn-On Time	t_{ON}	V_{DD} = 40V, I_D = 75A V_{GS} = 10V, R_{GS} = 3.9Ω (Figures 18, 19)	-	-	195	ns
Turn-On Delay Time	$t_{d(ON)}$		-	12.5	-	ns
Rise Time	t_r		-	117	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	-	ns
Fall Time	t_f		-	80	-	ns
Turn-Off Time	t_{OFF}		-	-	195	ns
GATE CHARGE SPECIFICATIONS						
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V; V_{DD} = 40V, I_D = 75A, $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	150	180	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V	-	80	96	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V	-	5.7	7	nC
Gate to Source Gate Charge	Q_{gs}		-	15	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	33	-	nC
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	2750	-	pF
Output Capacitance	C_{OSS}		-	700	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	250	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.25	V
		I_{SD} = 37.5A	-	-	1.00	V
Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	102	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	255	nC