HUF75345G3, HUF75345P3, HUF75345S3S

[redacted]

N-Channel UltraFET Power MOSFET
55 V, 75 A, 7 mΩ

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75345.

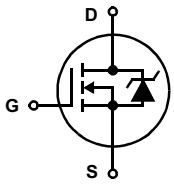
Features

- 75A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - Thermal Impedance SPICE and SABER Models Available on the WEB at: www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Ordering Information

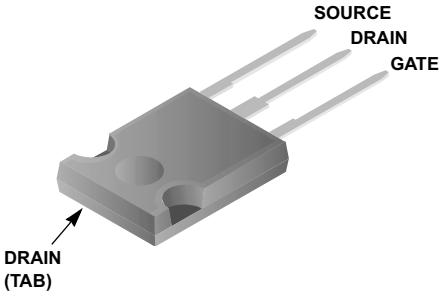
PART NUMBER	PACKAGE	BRAND
HUF75345G3	TO-247	75345G
HUF75345P3	TO-220AB	75345P
HUF75345S3ST	TO-263AB	75345S

Symbol

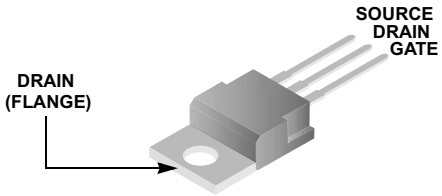


Packaging

JEDEC STYLE TO-247



JEDEC TO-220AB



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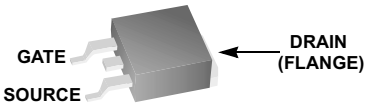

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	75	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figure 6	
Power Dissipation	P_D	325	W
Derate Above 25^oC		2.17	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		55	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 45V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figure 9)		-	0.006	0.007	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	0.46	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220, TO-263		-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \cong$ 75A, R_L = 0.4Ω, V_{GS} = 10V, R_{GS} = 2.5Ω		-	-	195	ns
Turn-On Delay Time	$t_{d(ON)}$			-	14	-	ns
Rise Time	t_r			-	118	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	42	-	ns
Fall Time	t_f			-	26	-	ns
Turn-Off Time	t_{OFF}			-	-	98	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 30V, $I_D \cong$ 75A, R_L = 0.4Ω $I_{g(REF)}$ = 1.0mA (Figure 13)	-	220	275	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	125	165	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	6.8	10	nC
Gate to Source Gate Charge	Q_{gs}			-	14	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	58	-	nC

Electrical Specifications T_C = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	4000	-	pF
Output Capacitance	C_{OSS}		-	1450	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	450	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	55	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	80	nC

Typical Performance Curves

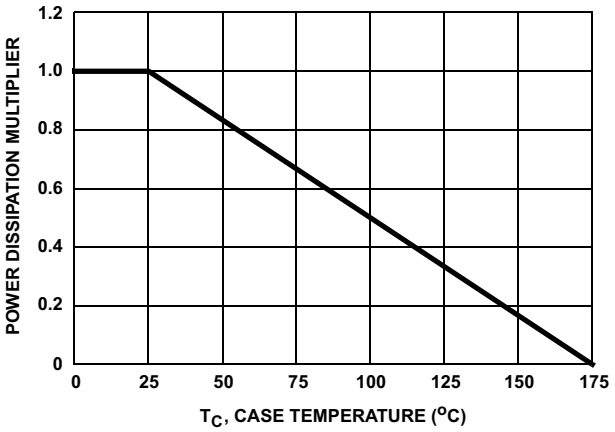

FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

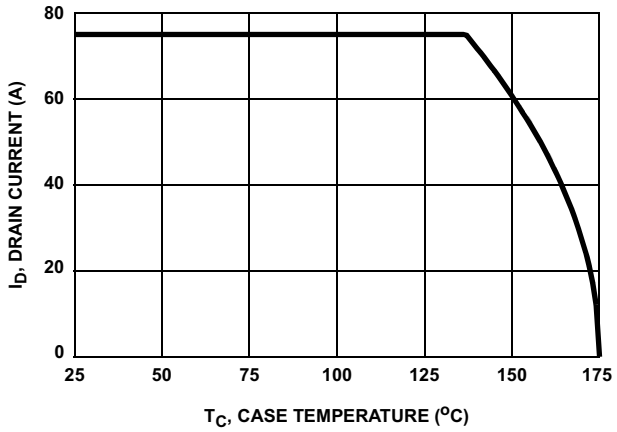

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

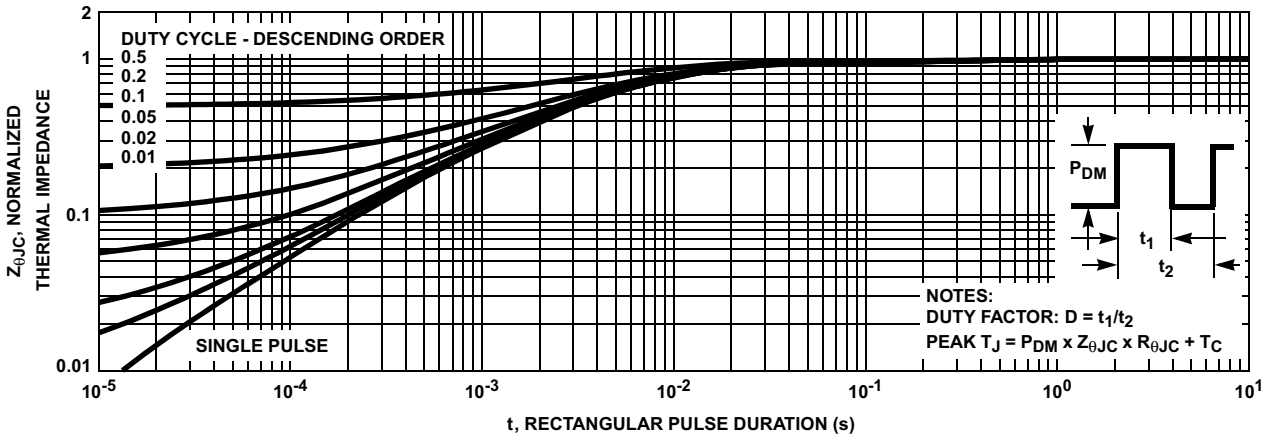

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE