



# HUF75344G3, HUF75344P3, HUF75344S3S

## 75A, 55V, 0.008 Ohm, N-Channel UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75344.

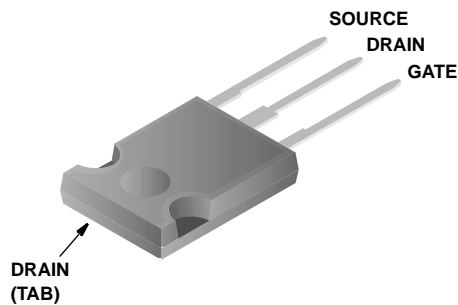
## Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75344G3	TO-247	75344G
HUF75344P3	TO-220AB	75344P
HUF75344S3S	TO-263AB	75344S

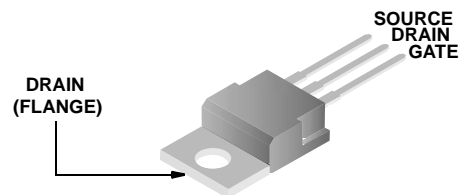
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75344S3ST.

## Packaging

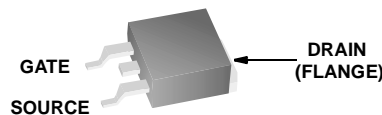
JEDEC STYLE TO-247



JEDEC TO-220AB



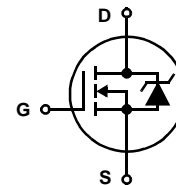
JEDEC TO-263AB



## Features

- 75A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - Thermal Impedance PSPICE and SABER Models Available on the web at: [www.fairchildsemi.com](http://www.fairchildsemi.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

## Symbol



# HUF75344G3, HUF75344P3, HUF75344S3S

## Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$	55 V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	55 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Drain Current		
Continuous (Figure 2) . . . . .	$I_D$	75 A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figure 6
Power Dissipation . . . . .	$P_D$	285 W
Derate Above $25^{\circ}\text{C}$ . . . . .		1.90 $\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	$-55$ to $175$ $^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $T_J = 25^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ .

## Electrical Specifications $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V	-	-	1	μA	
		V <sub>DS</sub> = 45V, V <sub>GS</sub> = 0V, T <sub>C</sub> = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r <sub>DS(ON)</sub>	I <sub>D</sub> = 75A, V <sub>GS</sub> = 10V (Figure 9)	-	6.5	8.0	mΩ	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R <sub>θJC</sub>	(Figure 3)	-	-	0.52	°C/W	
Thermal Resistance Junction to Ambient	R <sub>θJA</sub>	TO-247	-	-	30	°C/W	
		TO-220, TO-263	-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V <sub>GS</sub> = 10V)							
Turn-On Time	t <sub>ON</sub>	V <sub>DD</sub> = 30V, I <sub>D</sub> ≡ 75A, R <sub>L</sub> = 0.4Ω, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 3.0Ω	-	-	187	ns	
Turn-On Delay Time	t <sub>d(ON)</sub>		-	13	-	ns	
Rise Time	t <sub>r</sub>		-	125	-	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>		-	46	-	ns	
Fall Time	t <sub>f</sub>		-	57	-	ns	
Turn-Off Time	t <sub>OFF</sub>		-	-	147	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q <sub>g(TOT)</sub>	V <sub>GS</sub> = 0V to 20V	V <sub>DD</sub> = 30V, I <sub>D</sub> ≡ 75A, R <sub>L</sub> = 0.4Ω I <sub>g(REF)</sub> = 1.0mA (Figure 13)	-	175	210	nC
Gate Charge at 10V	Q <sub>g(10)</sub>	V <sub>GS</sub> = 0V to 10V		-	90	108	nC
Threshold Gate Charge	Q <sub>g(TH)</sub>	V <sub>GS</sub> = 0V to 2V		-	5.9	7.0	nC
Gate to Source Gate Charge	Q <sub>gs</sub>			-	14	-	nC
Reverse Transfer Capacitance	Q <sub>gd</sub>			-	39	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz (Figure 12)	-	3200	-	pF	
Output Capacitance	C <sub>OSS</sub>		-	1170	-	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	310	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 75A$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 75A, dI_{SD}/dt = 100A/\mu s$	-	-	105	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 75A, dI_{SD}/dt = 100A/\mu s$	-	-	210	nC

Typical Performance Curves

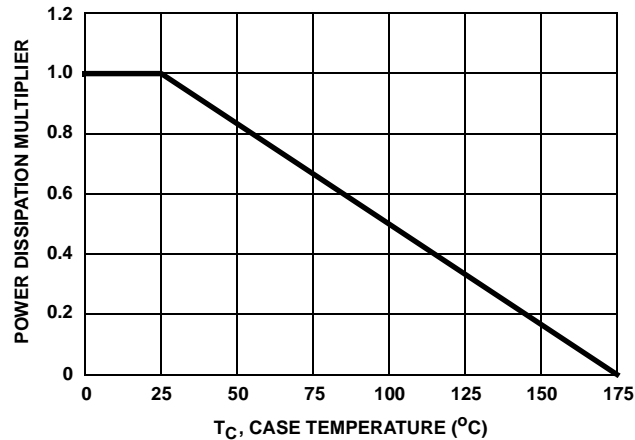


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

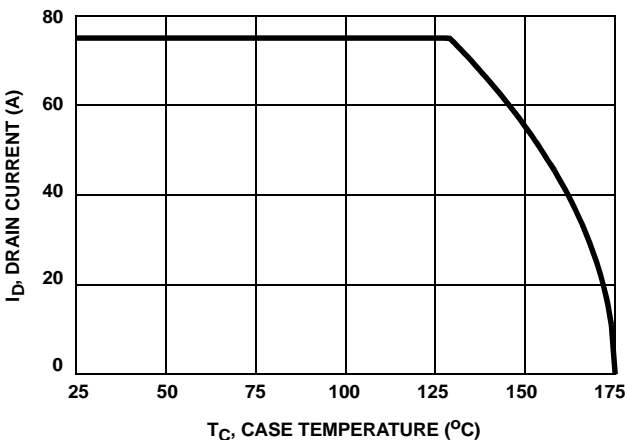


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

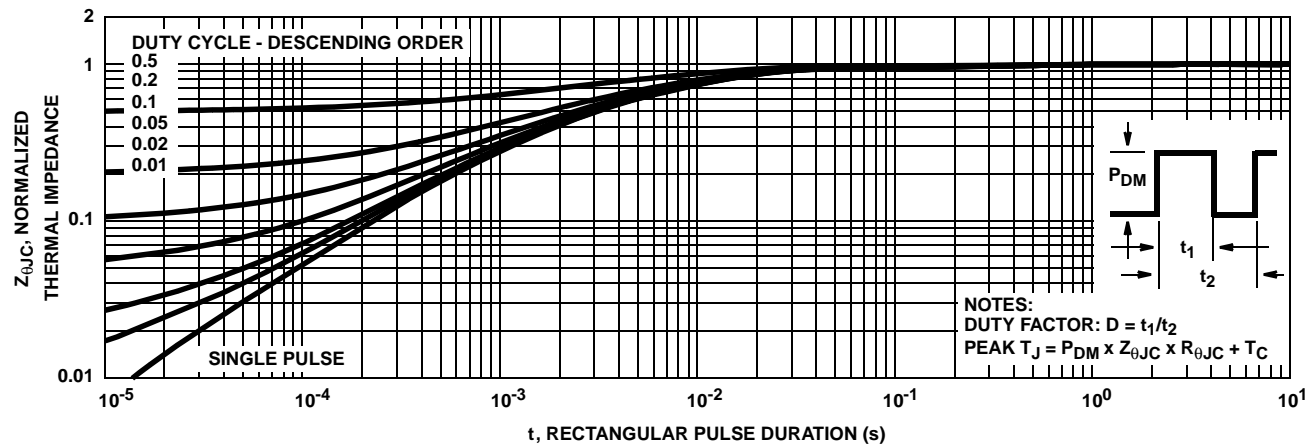


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE