

44A, 50V, 0.022 Ohm, N-Channel UltraFET Power MOSFET

This N-Channel power MOSFET is manufactured using the innovative UltraFET™ process. This advanced process technology achieves the

lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Ordering Information

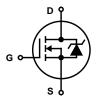
PART NUMBER	PACKAGE	BRAND		
HUF75229P3	TO-220AB	75229P		

NOTE: When ordering use the entire part number.

Features

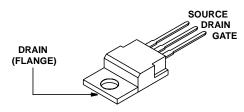
- 44A, 50V
- Low On-Resistance, r_{DS(ON)} = 0.022Ω
- Temperature Compensating PSPICE Model
- Thermal Impedance SPICE Model
- · Peak Current vs Pulse Width Curve
- UIS Rating Curve
- · Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



HUF75229P3

Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	50	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	50	V
Gate to Source Voltage	±20	V
Drain Current		
Continuous (Figure 2)	44	Α
Pulsed Drain Current	Figure 5	
Pulsed Avalanche Rating	Figure 6, 14, 15	
Power Dissipation	90	W
Derate Above 25°C	0.6	W/oC
Operating and Storage Temperature	-55 to 175	°С
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	οС
Package Body for 10s, See Techbrief 334	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}C$ to $150^{\circ}C$.

Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} =	50	-	-	V	
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 45V, V_{GS} = 0V$ $V_{DS} = 40V, V_{GS} = 0V, T_{C} = 150^{\circ}C$		-	-	1	μА
				-	-	250	μА
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 44A, V _{GS} = 10V (Figure 9)		0.017	0.020	0.022	Ω
Turn-On Time	ton	$V_{DD} = 30V, I_{D} \approx 44A,$ $R_{L} = 0.68\Omega, V_{GS} = 10V,$ $R_{GS} = 9.1\Omega$ (Figures 18, 19)		-	-	105	ns
Turn-On Delay Time	t _{d(ON)}			-	12	-	ns
Rise Time	t _r			-	58	-	ns
Turn-Off Delay Time	t _d (OFF)			-	33	-	ns
Fall Time	t _f			-	33	-	ns
Turn-Off Time	tOFF			-	-	100	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	$V_{DD} = 30V,$ $I_{D} \cong 44A,$ $R_{1} = 0.68\Omega$	-	60	75	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	35	43	nC
Threshold Gate Charge	Q _{g(TH)}	$V_{GS} = 0V \text{ to } 2V$	I _{g(REF)} = 1.0mA (Figures 13, 16, 17)	-	2.0	2.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)		-	1060	-	pF
Output Capacitance	Coss			-	405	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	95	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	1.66	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220		-	-	62	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V _{SD}	I _{SD} = 44A	-	-	1.25	V
Reverse Recovery Time	t _{rr}	$I_{SD} = 44A$, $dI_{SD}/dt = 100A/\mu s$	-	-	72	ns
Reverse Recovered Charge	Q _{RR}	$I_{SD} = 44A$, $dI_{SD}/dt = 100A/\mu s$	-	-	120	nC