



FQD2N100/FQU2N100

1000V N-Channel MOSFET

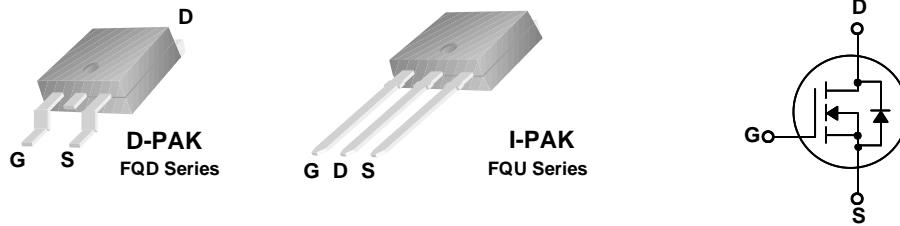
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp starter and ballast.

Features

- 1.6A, 1000V, $R_{DS(on)} = 9\Omega$ @ $V_{GS} = 10$ V
- Low gate charge (typical 12 nC)
- Low C_{rss} (typical 5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | FQD2N100/FQU2N100 | Units |
|----------------|--|-------------------|---------------------|
| V_{DSS} | Drain-Source Voltage | 1000 | V |
| I_D | Drain Current - Continuous ($T_c = 25^\circ\text{C}$) | 1.6 | A |
| | - Continuous ($T_c = 100^\circ\text{C}$) | 1.0 | A |
| I_{DM} | Drain Current - Pulsed | (Note 1) | A |
| V_{GSS} | Gate-Source Voltage | ± 30 | V |
| E_{AS} | Single Pulsed Avalanche Energy | (Note 2) | mJ |
| I_{AR} | Avalanche Current | (Note 1) | A |
| E_{AR} | Repetitive Avalanche Energy | (Note 1) | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | V/ns |
| P_D | Power Dissipation ($T_A = 25^\circ\text{C}$) * | 2.5 | W |
| | Power Dissipation ($T_c = 25^\circ\text{C}$) | 50 | W |
| | - Derate above 25°C | 0.4 | W/ $^\circ\text{C}$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |
| T_L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|-----------------|---|-----|-----|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 2.5 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | -- | 50 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 110 | $^\circ\text{C}/\text{W}$ |

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--|---|--|------|-------|------|---------------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$ | 1000 | -- | -- | V |
| $\Delta \text{BV}_{\text{DSS}} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, Referenced to 25°C | -- | 0.976 | -- | $\text{V}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{\text{DS}} = 1000 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$ | -- | -- | 10 | μA |
| | | $V_{\text{DS}} = 800 \text{ V}$, $T_C = 125^\circ\text{C}$ | -- | -- | 100 | μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{\text{GS}} = 30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$ | -- | -- | 100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{\text{GS}} = -30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$ | -- | -- | -100 | nA |

On Characteristics

| | | | | | | |
|---------------------|-----------------------------------|---|-----|-----|-----|----------|
| $V_{\text{GS(th)}}$ | Gate Threshold Voltage | $V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250 \mu\text{A}$ | 3.0 | -- | 5.0 | V |
| $R_{\text{DS(on)}}$ | Static Drain-Source On-Resistance | $V_{\text{GS}} = 10 \text{ V}$, $I_D = 0.8 \text{ A}$ | -- | 7.1 | 9 | Ω |
| g_{FS} | Forward Transconductance | $V_{\text{DS}} = 50 \text{ V}$, $I_D = 0.8 \text{ A}$ (Note 4) | -- | 1.9 | -- | S |

Dynamic Characteristics

| | | | | | | |
|------------------|------------------------------|---|----|-----|-----|----|
| C_{iss} | Input Capacitance | $V_{\text{DS}} = 25 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$ | -- | 400 | 520 | pF |
| C_{oss} | Output Capacitance | | -- | 40 | 52 | pF |
| C_{rss} | Reverse Transfer Capacitance | | -- | 5 | 6.5 | pF |

Switching Characteristics

| | | | | | | |
|---------------------|---------------------|---|----|-----|------|----|
| $t_{\text{d(on)}}$ | Turn-On Delay Time | $V_{\text{DD}} = 500 \text{ V}$, $I_D = 2.0 \text{ A}$, $R_G = 25 \Omega$ | -- | 13 | 35 | ns |
| t_r | Turn-On Rise Time | | -- | 30 | 70 | ns |
| $t_{\text{d(off)}}$ | Turn-Off Delay Time | | -- | 25 | 60 | ns |
| t_f | Turn-Off Fall Time | | -- | 35 | 80 | ns |
| Q_g | Total Gate Charge | | -- | 12 | 15.5 | nC |
| Q_{gs} | Gate-Source Charge | $V_{\text{DS}} = 800 \text{ V}$, $I_D = 2.0 \text{ A}$, $V_{\text{GS}} = 10 \text{ V}$ | -- | 2.5 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | -- | 6.5 | -- | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|-----------------|---|--|----|-----|-----|---------------|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | -- | -- | 1.5 | A | |
| I_{SM} | Maximum Pulsed Drain-Source Diode Forward Current | -- | -- | 6.0 | A | |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{\text{GS}} = 0 \text{ V}$, $I_S = 1.6 \text{ A}$ | -- | -- | 1.4 | V |
| t_{rr} | Reverse Recovery Time | $V_{\text{GS}} = 0 \text{ V}$, $I_S = 2.0 \text{ A}$, $dI_F / dt = 100 \text{ A}/\mu\text{s}$ | -- | 520 | -- | ns |
| Q_{rr} | Reverse Recovery Charge | | -- | 2.3 | -- | μC |

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 120\text{mH}$, $I_{AS} = 1.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 2.0\text{A}$, $dI/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq \text{BV}_{\text{DSS}}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

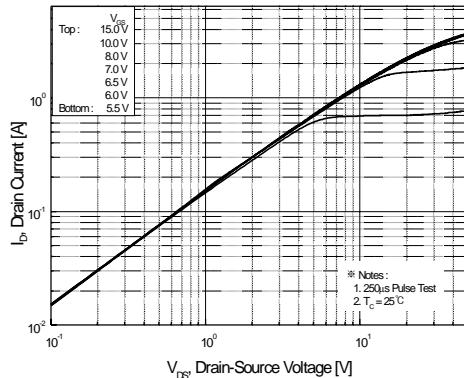


Figure 1. On-Region Characteristics

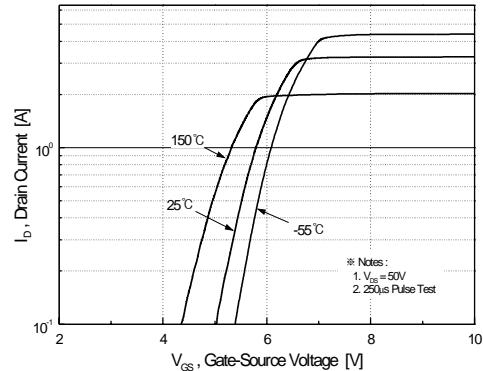


Figure 2. Transfer Characteristics

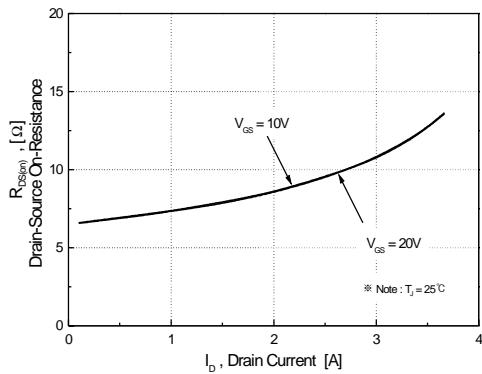


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

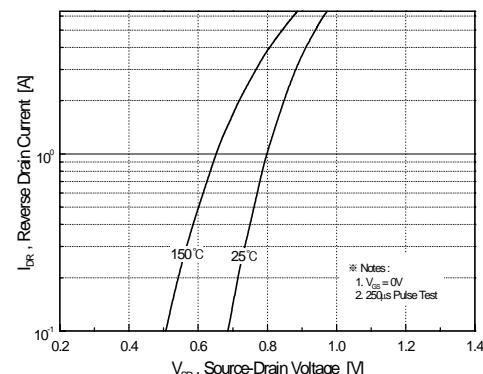


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

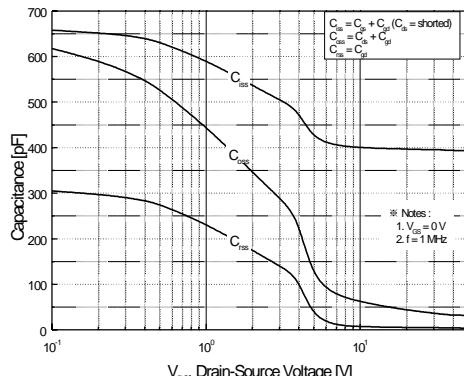


Figure 5. Capacitance Characteristics

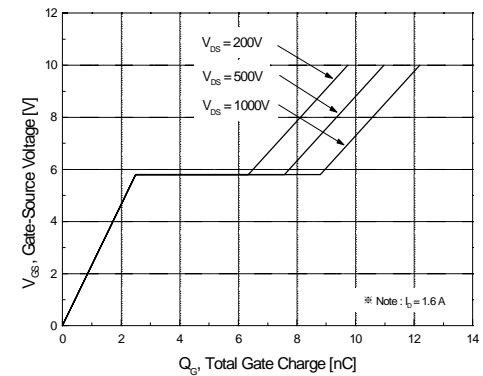


Figure 6. Gate Charge Characteristics