

FQB19N20L / FQI19N20L

200V LOGIC N-Channel MOSFET

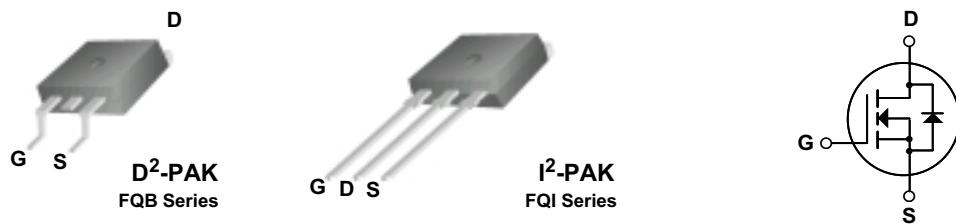
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply, motor control.

Features

- 21A, 200V, $R_{DS(on)} = 0.14\Omega$ @ $V_{GS} = 10$ V
- Low gate charge (typical 27 nC)
- Low C_{rss} (typical 30 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirement allowing direct operation from logic drivers



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB19N20L / FQI19N20L	Units
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	21	A
	- Continuous ($T_C = 100^\circ\text{C}$)	13.3	A
I_{DM}	Drain Current - Pulsed	(Note 1)	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	140	W
	- Derate above 25°C	1.12	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.89	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta CA}$	Thermal Resistance, Case-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.16	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	1	μA
		$V_{DS} = 160 \text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0	--	2.0	V
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 10.5 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 10.5 \text{ A}$ (Note 4)	-- --	0.11 0.12	0.14 0.15	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 30 \text{ V}, I_D = 10.5 \text{ A}$	--	18.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	--	1700	2200	pF
C_{oss}	Output Capacitance		--	220	290	pF
C_{rss}	Reverse Transfer Capacitance		--	30	40	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100 \text{ V}, I_D = 21 \text{ A}, R_G = 25 \Omega$ (Note 4, 5)	--	35	80	ns
t_r	Turn-On Rise Time		--	300	610	ns
$t_{d(off)}$	Turn-Off Delay Time		--	130	270	ns
t_f	Turn-Off Fall Time		--	180	370	ns
Q_g	Total Gate Charge	$V_{DS} = 160 \text{ V}, I_D = 21 \text{ A}, V_{GS} = 5 \text{ V}$ (Note 4, 5)	--	27	35	nC
Q_{gs}	Gate-Source Charge		--	5.8	--	nC
Q_{gd}	Gate-Drain Charge		--	11.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	21	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	84	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 21 \text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = 21 \text{ A}$ $dI_F / dt = 100 \text{ A}/\mu\text{s}$	-- --	140 0.66	-- --	ns μC
Q_{rr}	Reverse Recovery Charge					

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.85\text{mH}$, $I_{AS} = 21\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 21\text{A}$, $dI/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

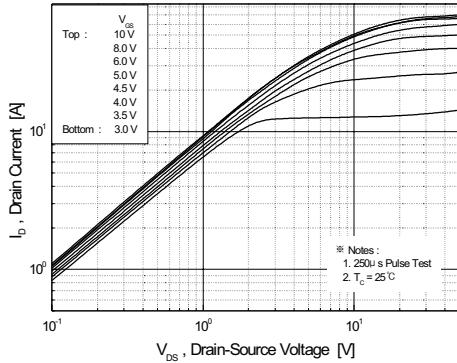


Figure 1. On-Region Characteristics

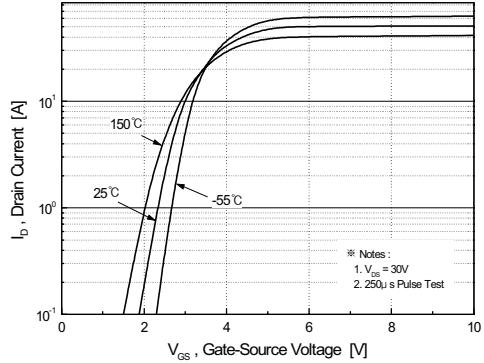


Figure 2. Transfer Characteristics

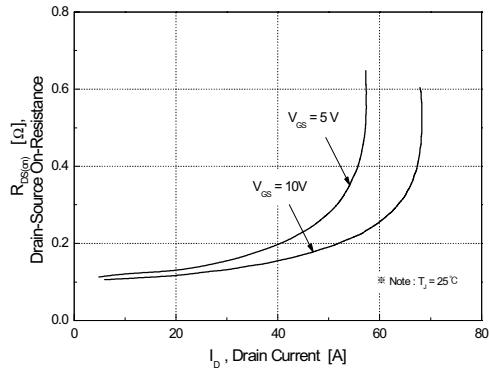


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

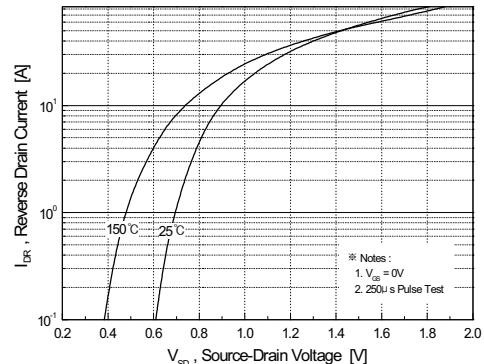


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

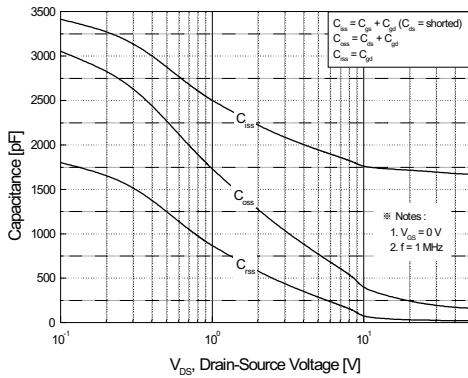


Figure 5. Capacitance Characteristics

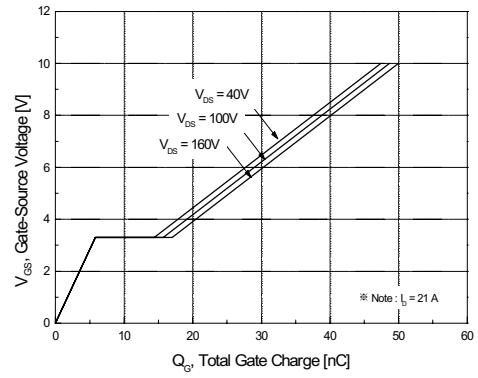


Figure 6. Gate Charge Characteristics