



# FQB12N50 / FQI12N50

## 500V N-Channel MOSFET

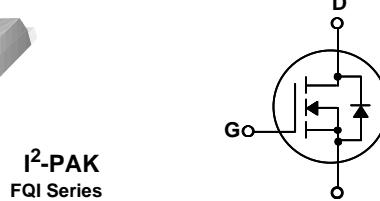
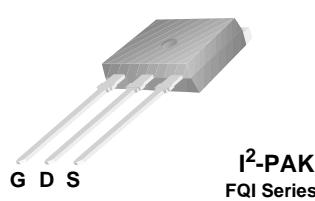
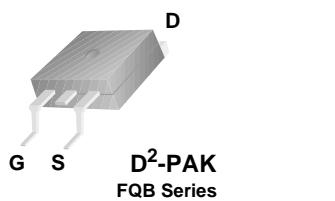
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction, electronic lamp ballasts based on half bridge.

### Features

- 12.1A, 500V,  $R_{DS(on)} = 0.49\Omega$  @  $V_{GS} = 10$  V
- Low gate charge ( typical 39 nC)
- Low  $C_{RSS}$  ( typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	FQB12N50 / FQI12N50	Units
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	12.1	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	7.6	A
$I_{DM}$	Drain Current - Pulsed	(Note 1)	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$I_{AR}$	Avalanche Current	(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	179	W
	- Derate above $25^\circ\text{C}$	1.43	W/ $^\circ\text{C}$
$T_J, T_{stg}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta CA}$	Thermal Resistance, Case-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	500	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.48	--	$\text{V}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 500 \text{ V}$ , $V_{\text{GS}} = 0 \text{ V}$	--	--	1	$\mu\text{A}$
		$V_{\text{DS}} = 400 \text{ V}$ , $T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{\text{GSSF}}$	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 30 \text{ V}$ , $V_{\text{DS}} = 0 \text{ V}$	--	--	100	nA
$I_{\text{GSSR}}$	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -30 \text{ V}$ , $V_{\text{DS}} = 0 \text{ V}$	--	--	-100	nA

## On Characteristics

$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250 \mu\text{A}$	3.0	--	5.0	V
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10 \text{ V}$ , $I_D = 6.05 \text{ A}$ (Note 4)	--	0.39	0.49	$\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = 50 \text{ V}$ , $I_D = 6.05 \text{ A}$	--	9.8	--	S

## Dynamic Characteristics

$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 25 \text{ V}$ , $V_{\text{GS}} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$	--	1550	2020	pF
$C_{\text{oss}}$	Output Capacitance		--	220	285	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		--	25	33	pF

## Switching Characteristics

$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 250 \text{ V}$ , $I_D = 12.1 \text{ A}$ , $R_G = 25 \Omega$ (Note 4,5)	--	35	80	ns
$t_r$	Turn-On Rise Time		--	120	250	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	70	150	ns
$t_f$	Turn-Off Fall Time		--	80	170	ns
$Q_g$	Total Gate Charge	$V_{\text{DS}} = 400 \text{ V}$ , $I_D = 12.1 \text{ A}$ , $V_{\text{GS}} = 10 \text{ V}$ (Note 4,5)	--	39	51	nC
$Q_{\text{gs}}$	Gate-Source Charge		--	9.3	--	nC
$Q_{\text{gd}}$	Gate-Drain Charge		--	17.4	--	nC

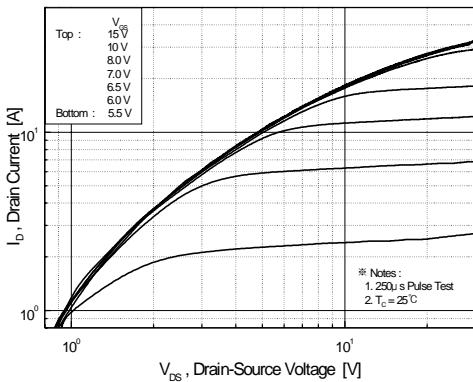
## Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	12.1	A	
$I_{\text{SM}}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	48.4	A	
$V_{\text{SD}}$	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_S = 12.1 \text{ A}$	--	--	1.4	V
$t_{\text{rr}}$	Reverse Recovery Time	$V_{\text{GS}} = 0 \text{ V}$ , $I_S = 12.1 \text{ A}$ , $dI_F / dt = 100 \text{ A}/\mu\text{s}$	--	300	--	ns
$Q_{\text{rr}}$	Reverse Recovery Charge	$V_{\text{GS}} = 0 \text{ V}$ , $I_S = 12.1 \text{ A}$ , $dI_F / dt = 100 \text{ A}/\mu\text{s}$ (Note 4)	--	2.6	--	$\mu\text{C}$
			--			

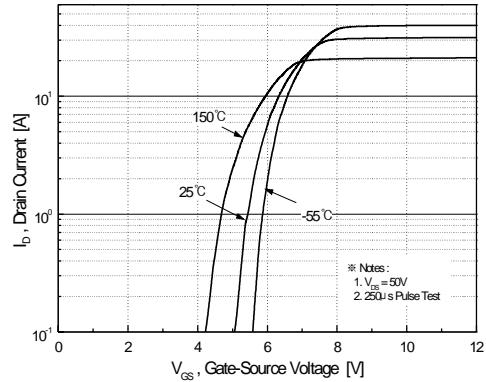
### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 10.8\text{mH}$ ,  $I_{AS} = 12.1\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 12.1\text{A}$ ,  $dI/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq \text{BV}_{\text{DSS}}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

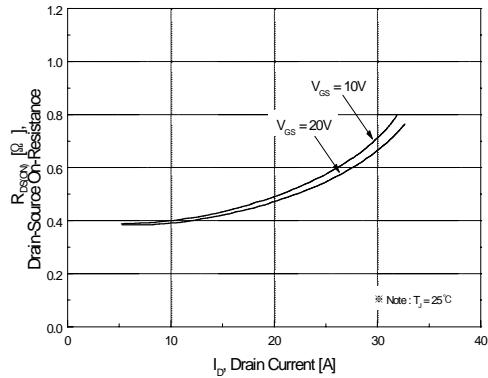
## Typical Characteristics



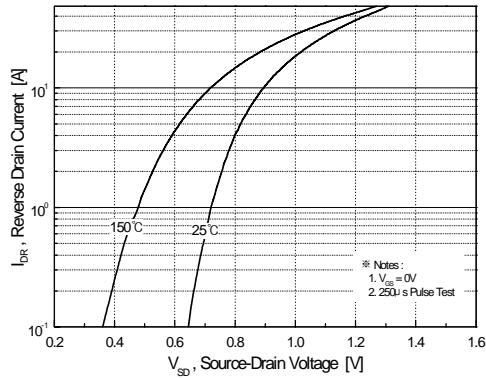
**Figure 1. On-Region Characteristics**



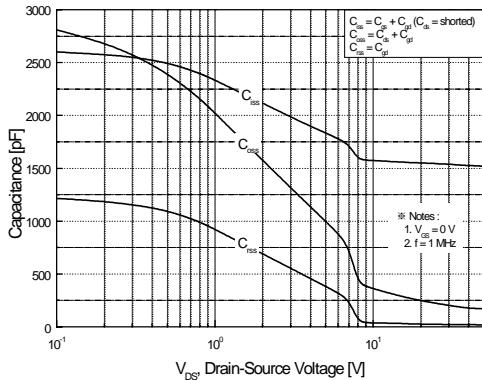
**Figure 2. Transfer Characteristics**



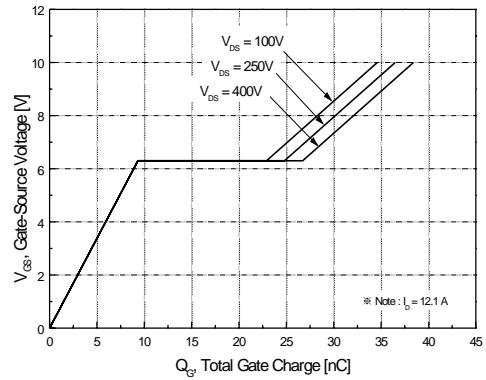
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**