

FDD6680A/FDU6680A

30V N-Channel PowerTrench[®] MOSFET

General Description

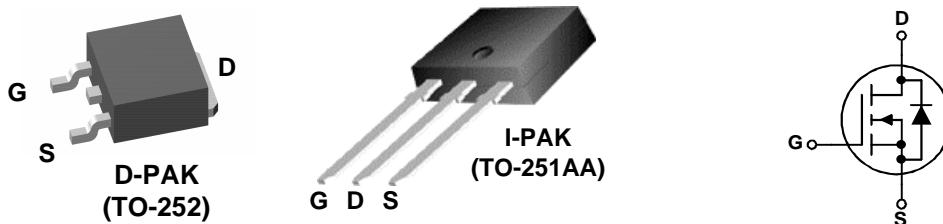
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and extremely low $R_{DS(ON)}$ in a small package.

Applications

- DC/DC converter
- Motor Drives

Features

- 56 A, 30 V $R_{DS(ON)} = 9.5 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 13 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge
- Fast Switching
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings		Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage	± 20		V
I_D	Continuous Drain Current @ $T_C=25^\circ\text{C}$	56		A
	@ $T_A=25^\circ\text{C}$	14		
	Pulsed	100		
P_D	Power Dissipation @ $T_C=25^\circ\text{C}$	60		W
	@ $T_A=25^\circ\text{C}$	2.8		
	@ $T_A=25^\circ\text{C}$	1.3		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +175		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	2.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	45	
$R_{\theta JA}$		(Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6680A	FDD6680A	D-PAK (TO-252)	13"	12mm	2500 units
FDU6680A	FDU6680A	I-PAK (TO-251)	Tube	N/A	75

Electrical Characteristics						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
E_{AS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15$ V, $I_D = 14$ A			174	mJ
I_{AS}	Drain-Source Avalanche Current				14	A
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μ A	30			V
ΔBV_{DSS} ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μ A, Referenced to 25°C		26		mV/°C
I_{BSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V			1	μ A
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1	1.8	3	V
$\Delta V_{GS(th)}$ ΔT_J	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ μ A, Referenced to 25°C		-5		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 14$ A $V_{GS} = 4.5$ V, $I_D = 12$ A $V_{GS} = 10$ V, $I_D = 14$ A, $T_J = 125$ °C	7 10 11	9.5 13 16		mΩ
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10$ V, $V_{DS} = 5$ V	50			A
g_F	Forward Transconductance	$V_{DS} = 10$ V, $I_D = 14$ A		56		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1.0$ MHz		1425		pF
C_{oss}	Output Capacitance			350		pF
C_{rss}	Reverse Transfer Capacitance			150		pF
R_G	Gate Resistance	$V_{osc} = 15$ mV, $f = 1.0$ MHz		1.3		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10$ V, $R_{GEN} = 6$ Ω		11	20	ns
t_r	Turn-On Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			31	50	ns
t_f	Turn-Off Fall Time			13	23	ns
Q_g	Total Gate Charge	$V_{DS} = 15$ V, $I_D = 14$ A, $V_{GS} = 5$ V		14	20	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			5		nC

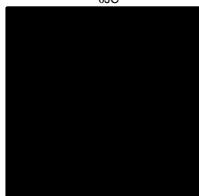
Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current			2.3		A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 2.3 \text{ A}$ (Note 2)	0.74	1.2		V
t_{rr}	Diode Reverse Recovery Time	$I_F = 14 \text{ A}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$	23			nS
Q_{rr}	Diode Reverse Recovery Charge		11			nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 45^\circ\text{C}/\text{W}$ when mounted on a
1in² pad of 2 oz copper



b) $R_{\theta JA} = 96^\circ\text{C}/\text{W}$ when mounted
on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

- Maximum current is calculated as:
$$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where P_D is maximum power dissipation at $T_C = 25^\circ\text{C}$ and $R_{DS(ON)}$ is at $T_{J(\text{max})}$ and $V_{GS} = 10\text{V}$. Package current limitation is 21A

Typical Characteristics

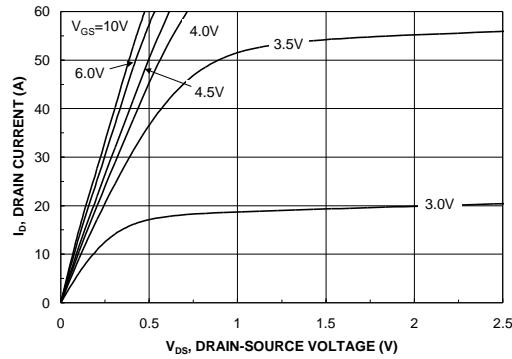


Figure 1. On-Region Characteristics

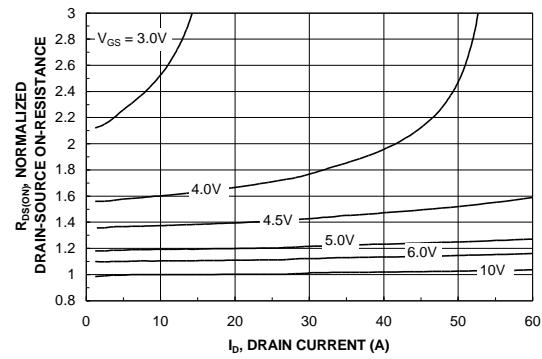


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

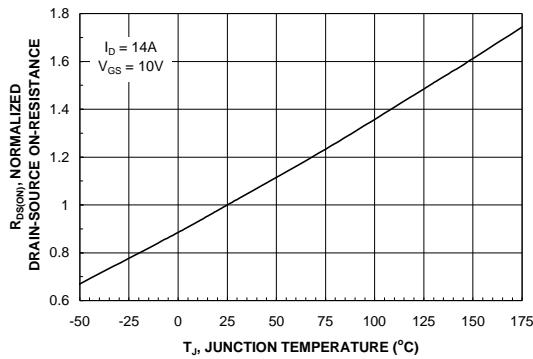


Figure 3. On-Resistance Variation with Temperature

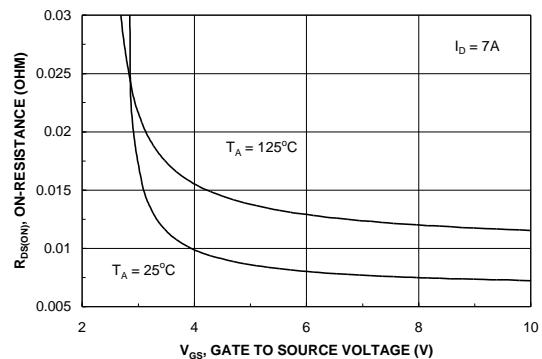


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

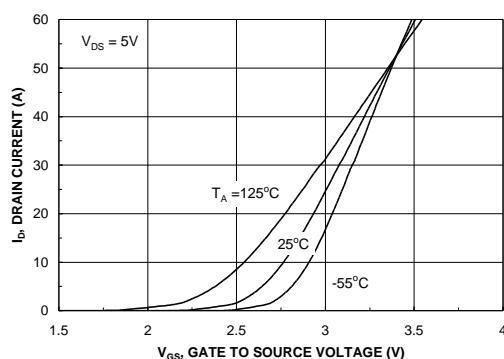


Figure 5. Transfer Characteristics

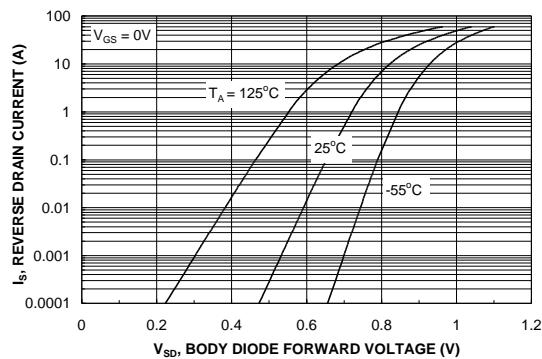


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature