

FDP7N60NZ / FDPF7N60NZ

N-Channel UniFET™ II MOSFET

600 V, 6.5 A, 1.25 Ω

Features

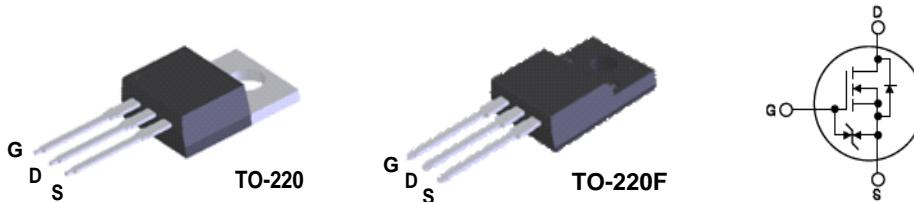
- $R_{DS(on)} = 1.05 \Omega$ (Typ.) @ $V_{GS} = 10$ V, $I_D = 3.25$ A
- Low Gate Charge (Typ. 13 nC)
- Low C_{RSS} (Typ. 7 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ II MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter		FDP7N60NZ	FDPF7N60NZ	Unit
V_{DSS}	Drain to Source Voltage		600		V
V_{GSS}	Gate to Source Voltage		± 30		V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	6.5	6.5*	A
		- Continuous ($T_C = 100^\circ\text{C}$)	3.9	3.9*	
I_{DM}	Drain Current	- Pulsed (Note 1)	26	26*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		275		mJ
I_{AR}	Avalanche Current (Note 1)		6.5		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		14.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		10		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	147	33	W	$^\circ\text{C}$
		- Derate above 25°C	1.2	0.26	
T_J , T_{STG}	Operating and Storage Temperature Range		-55 to +150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP7N60NZ	FDPF7N60NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.85	3.8	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case to Sink, Typ.	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP7N60NZ	FDP7N60NZ	TO-220	-	-	50
FDPF7N60NZ	FDPF7N60NZ	TO-220F	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	600	-	-	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	-	0.6	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 480\text{V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3	-	5	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 3.25\text{A}$	-	1.05	1.25	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 3.25\text{A}$	-	7.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	550	730	pF
C_{oss}	Output Capacitance		-	70	90	pF
C_{rss}	Reverse Transfer Capacitance		-	7	10	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V	$V_{DS} = 480\text{V}, I_D = 6.5\text{A}$ $V_{GS} = 10\text{V}$	-	13	17	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	5.6	nC

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 300\text{V}, I_D = 6.5\text{A}$ $R_G = 25\Omega$	-	17.5	45	ns
t_r	Turn-On Rise Time		-	30	70	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	40	90	ns
t_f	Turn-Off Fall Time		(Note 4)	-	25	60

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	6.5	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	26	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 6.5\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 6.5\text{A}$	-	250	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt = 100\text{A}/\mu\text{s}$	-	1.4	-	μC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 13\text{mH}, I_{AS} = 6.5\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 6.5\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq \text{BV}_{\text{DSS}}$, Starting $T_J = 25^\circ\text{C}$
- 4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

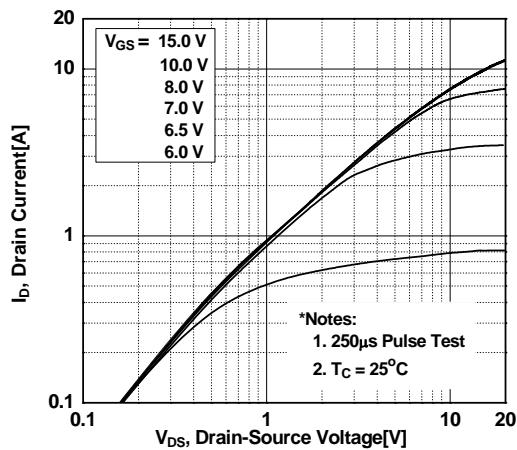


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

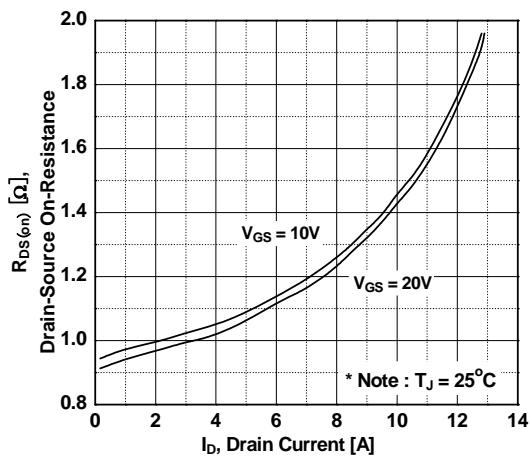


Figure 5. Capacitance Characteristics

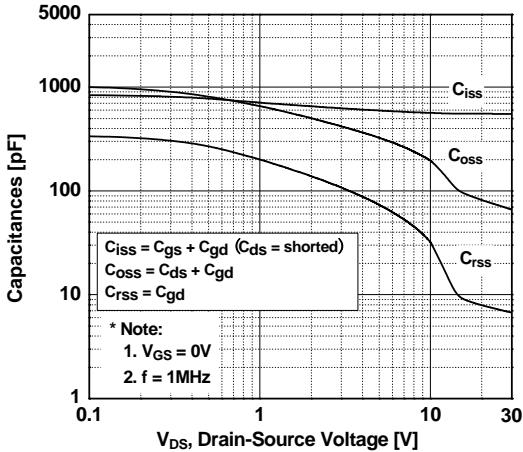


Figure 2. Transfer Characteristics

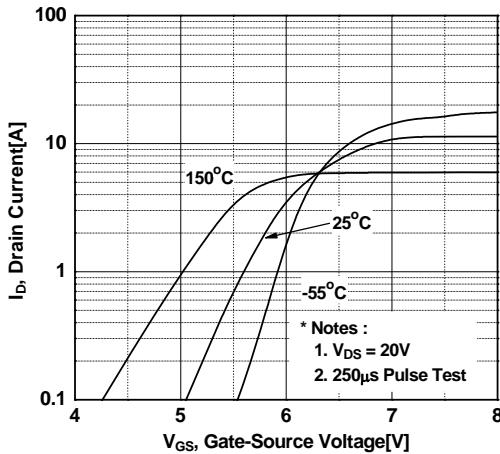


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

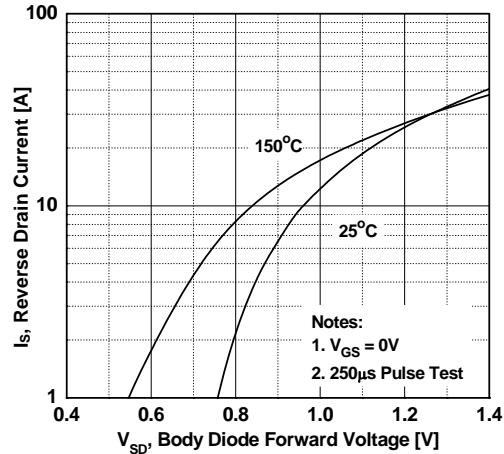


Figure 6. Gate Charge Characteristics

