

FDD6N50F / FDU6N50F

N-Channel MOSFET

500V, 5.5A, 1.15Ω

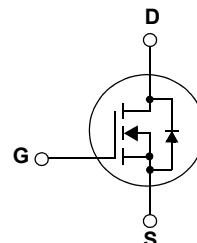
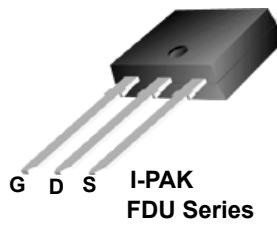
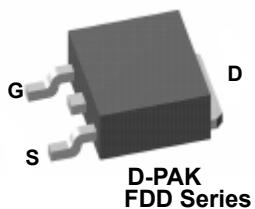
Features

- $R_{DS(on)} = 1.0\Omega$ (Typ.) @ $V_{GS} = 10V$, $I_D = 2.75A$
- Low gate charge (Typ. 15nC)
- Low C_{rss} (Typ. 6.3pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted*

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		± 30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ C$)	5.5	A
		-Continuous ($T_C = 100^\circ C$)	2.4	
I_{DM}	Drain Current	- Pulsed (Note 1)	22	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		270	mJ
I_{AR}	Avalanche Current (Note 1)		5.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		8.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ C$)	89	W	$W/^\circ C$
		- Derate above $25^\circ C$	0.71	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	83	

*When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6N50F	FDD6N50FTM	D-PAK	380mm	16mm	2500
FDD6N50F	FDD6N50FTF	D-PAK	380mm	16mm	2000
FDU6N50F	FDU6N50FTU	I-PAK	-	-	70

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

V_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta V_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	-	0.15	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	-	-	10	μA
		$V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.75\text{A}$	-	1.0	1.15	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}, I_D = 2.75\text{A}$ (Note 4)	-	4.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	720	960	pF
C_{oss}	Output Capacitance		-	85	115	pF
C_{rss}	Reverse Transfer Capacitance		-	6.3	9.5	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 6\text{A}$ $V_{GS} = 10\text{V}$	-	15	19.8	nC
Q_{gs}	Gate to Source Gate Charge		-	4.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4, 5)	-	6.1	nC

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 6\text{A}$ $R_G = 25\Omega$	-	17	44	ns
t_r	Turn-On Rise Time		-	28.3	66.6	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	33.4	76.7	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	-	20.5	51

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	5.5	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	22	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 5.5\text{A}$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 5.5\text{A}$ $dI_F/dt = 100\text{A}/\mu\text{s}$	-	85	-	ns
Q_{rr}	Reverse Recovery Charge		(Note 4)	-	0.15	μC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 16\text{mH}, I_{AS} = 5.5\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 5.5\text{A}, dI/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- 5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

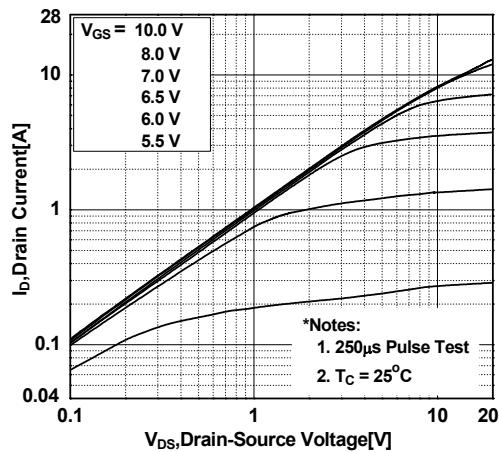


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

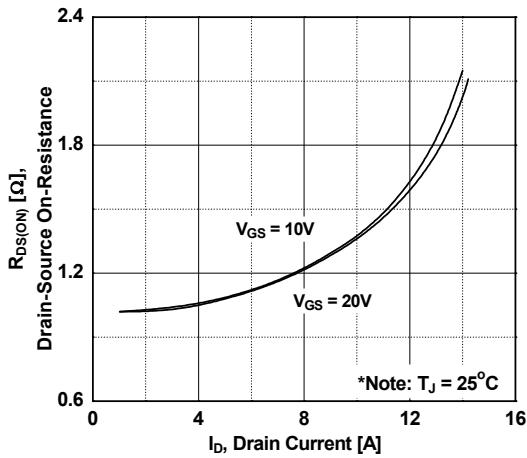


Figure 5. Capacitance Characteristics

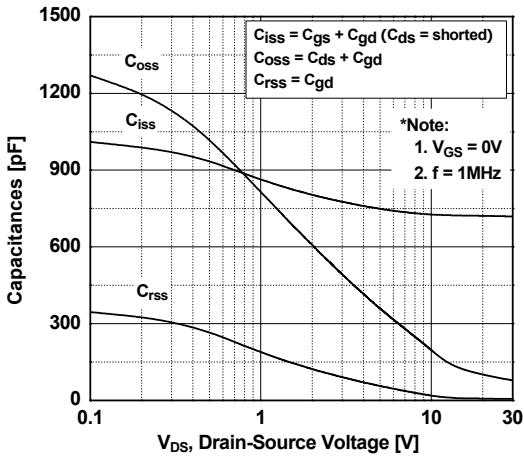


Figure 2. Transfer Characteristics

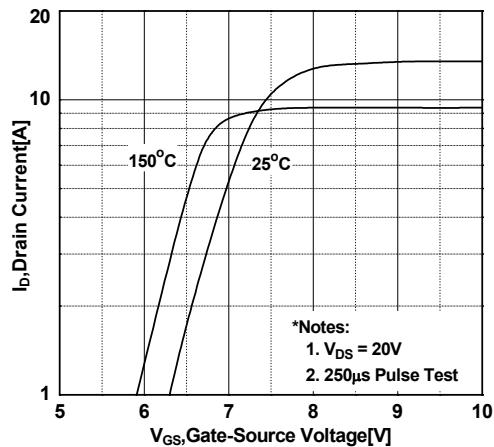


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

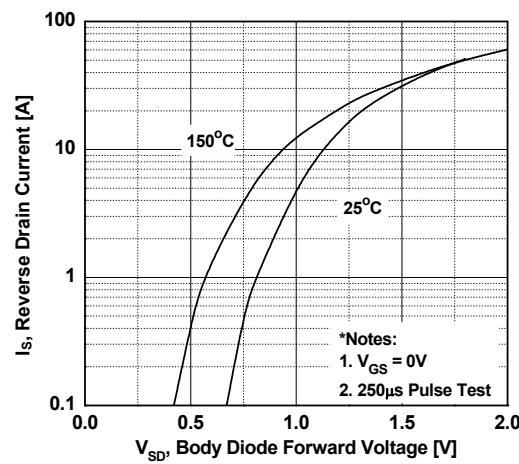


Figure 6. Gate Charge Characteristics

