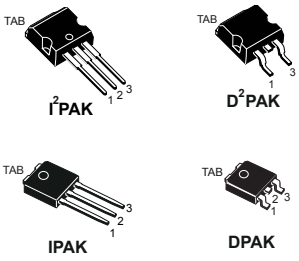
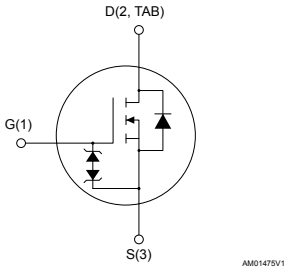
STB4NK60Z-1, STB4NK60ZT4
STD4NK60Z-1, STD4NK60ZT4

Datasheet

N-channel 600 V, 1.7 Ω typ., 4 A Power MOSFETs in I²PAK, D²PAK, IPAK and DPAK packages





Product status
STB4NK60Z-1
STB4NK60ZT4
STD4NK60Z-1
STD4NK60ZT4

Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	P_{TOT}	I_D
STB4NK60Z-1	600 V	2 Ω	70 W	4 A
STB4NK60ZT4				
STD4NK60Z-1				
STD4NK60ZT4				

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the technology by an optimization of the well-established. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	4	A
I_D	Drain current (continuous) at T_C = 100 °C	2.5	A
I_{DM} (1)	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
ESD	Gate-source human body model (C=100 pF, R=1.5 kΩ)	3	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 4 A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		I^2PAK, D^2PAK	IPAK, DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction- case	1.79		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	100	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	120	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2 A		1.7	2	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	510		pF
C_{oss}	Output capacitance			67		
C_{rss}	Reverse transfer capacitance			13		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 V to 480 V	-	38.5		
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 2 A,R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times)	-	12		ns
t_r	Rise time			9.5		
$t_{d(off)}$	Turn-off delay time			29		
t_f	Fall time			16.5		
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 480 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V) (see Figure 15. Test circuit for inductive load switching and diode recovery times)		12		
t_r	Fall time			12		
t_c	Cross-over time			19.5		
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 4 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	18.8	26	nC
Q_{gs}	Gate-source charge			3.8		
Q_{gd}	Gate-drain charge			9.8		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS}increases from 0 to 80% V_{DSS}.*

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM}	Source-drain current (pulsed)		-		16	
V_{SD}	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs	-	400		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 24 V, T_j = 150 °C	-	1.7		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8.5		A

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

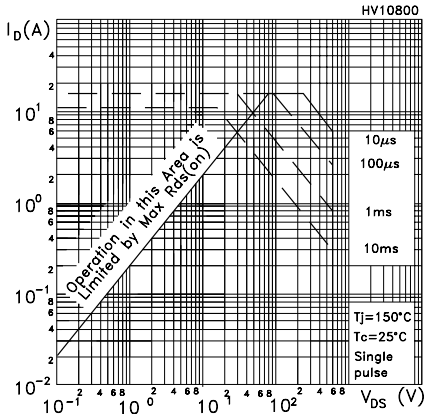


Figure 2. Thermal impedance

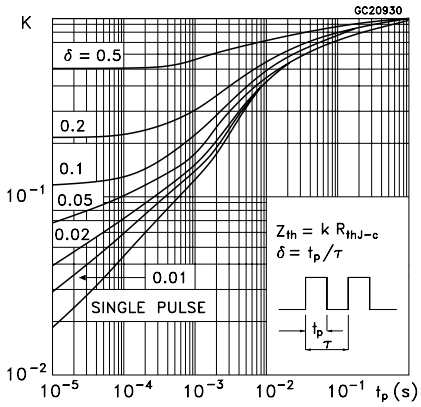


Figure 3. Output characterisics

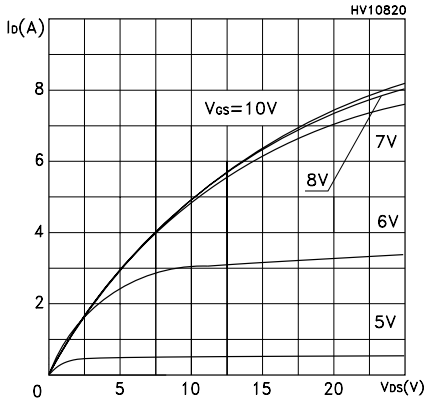


Figure 4. Transfer characteristics

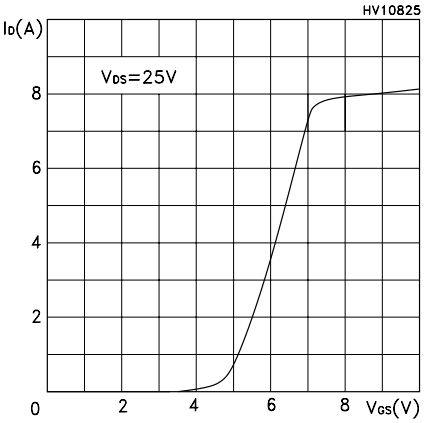


Figure 5. Static drain-source on-resistance

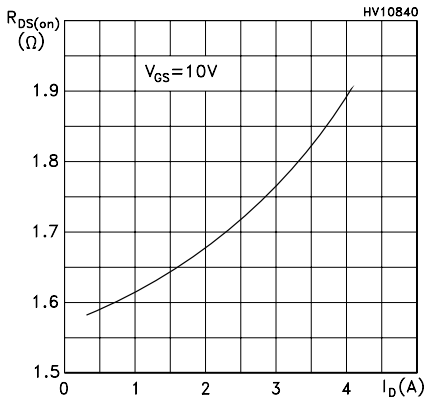


Figure 6. Gate charge vs gate-source voltage

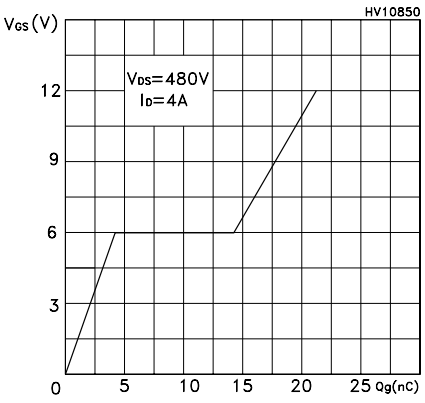


Figure 7. Capacitance variations

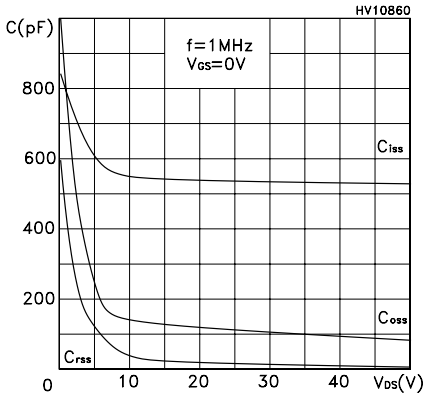


Figure 8. Normalized gate threshold voltage vs temperature

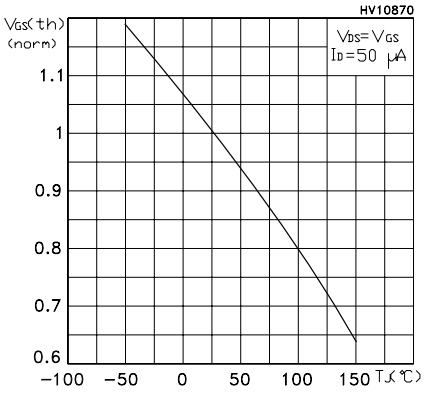


Figure 9. Normalized on-resistance vs temperature

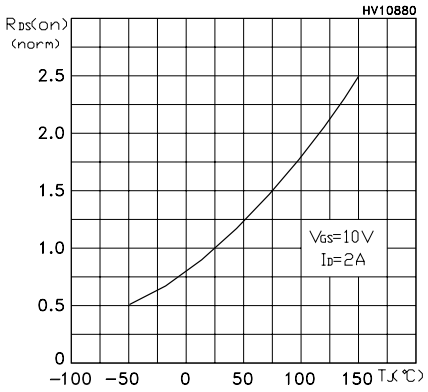


Figure 10. Source-drain diode forward characteristic

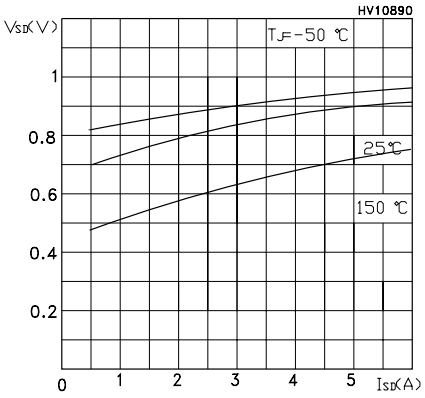


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

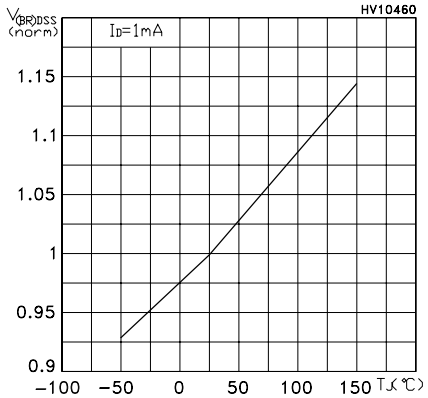
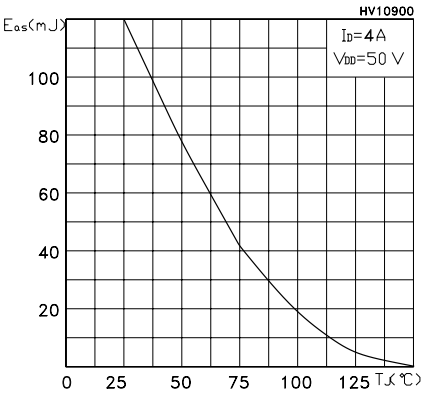


Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

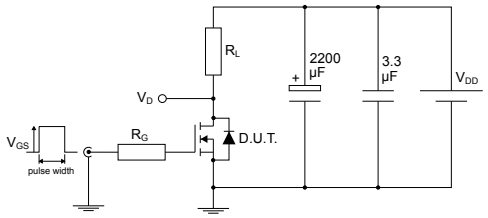


Figure 14. Test circuit for gate charge behavior

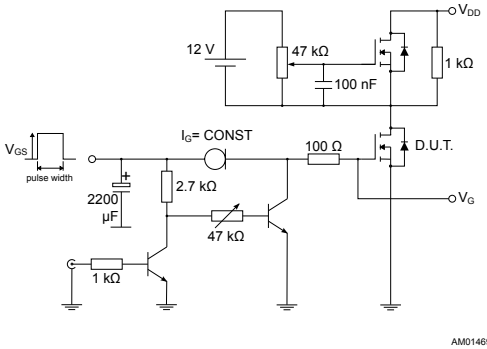


Figure 15. Test circuit for inductive load switching and diode recovery times

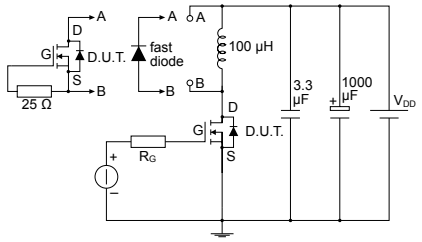


Figure 16. Unclamped inductive load test circuit

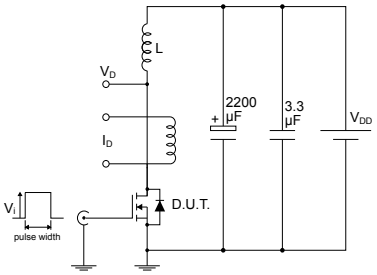


Figure 17. Unclamped inductive waveform

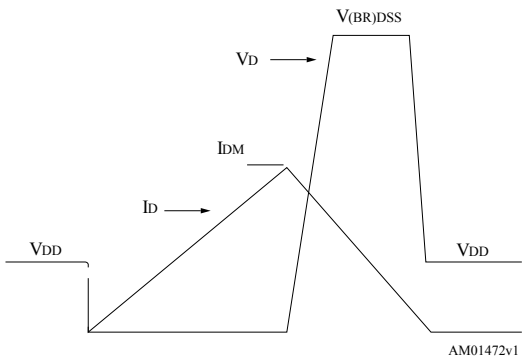


Figure 18. Switching time waveform