

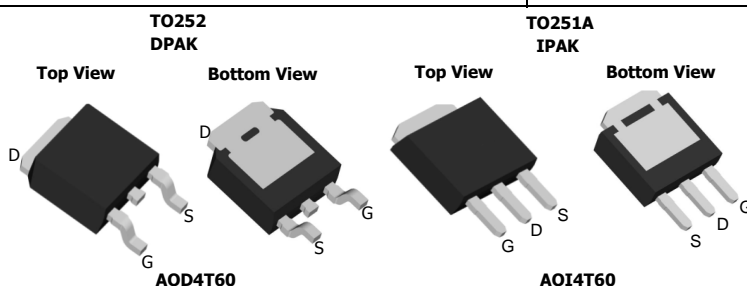
### General Description

The AOD4T60 & AOI4T60 are fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low  $R_{DS(on)}$ ,  $C_{iss}$  and  $C_{rss}$  along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

### Product Summary

$V_{DS} @ T_{j,max}$	700V
$I_{DM}$	16A
$R_{DS(ON),max}$	< 2.1 $\Omega$
$Q_{g,typ}$	9nC
$E_{oss} @ 400V$	1.6 $\mu$ J

100% UIS Tested!  
100%  $R_g$  Tested!



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain Current <sup>B</sup>	$I_D$	$T_C=25^\circ\text{C}$	4
		$T_C=100^\circ\text{C}$	2.5
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	16	A
Avalanche Current <sup>C,K</sup>	$I_{AR}$	4	A
Repetitive avalanche energy <sup>C,K</sup>	$E_{AR}$	8	mJ
Single pulsed avalanche energy <sup>H</sup>	$E_{AS}$	145	mJ
MOSFET $dv/dt$ ruggedness	$dv/dt$	50	V/ns
Peak diode recovery $dv/dt$		5	V/ns
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	83
		Derate above $25^\circ\text{C}$	0.7
Junction and Storage Temperature Range	$T_J, T_{STG}$	-50 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	$T_L$	300	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient <sup>A,G</sup>	$R_{\theta JA}$	40	50	$^\circ\text{C}/\text{W}$
Maximum Case-to-sink <sup>A</sup>	$R_{\theta CS}$	-	0.5	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case <sup>D,F</sup>	$R_{\theta JC}$	1.25	1.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>STATIC PARAMETERS</b>							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	600			V	
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C		700			
BV <sub>DSS</sub> /ΔT <sub>J</sub>	Zero Gate Voltage Drain Current	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V		0.6		V/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V			1	μA	
		V <sub>DS</sub> =480V, T <sub>J</sub> =125°C			10		
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V			±100	nA	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	3	4.2	5	V	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =1A		1.75	2.1	Ω	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =40V, I <sub>D</sub> =2A		2.8		S	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.79	1	V	
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4	A	
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current <sup>C</sup>				16	A	
<b>DYNAMIC PARAMETERS</b>							
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz		460		pF	
C <sub>oss</sub>	Output Capacitance				22		pF
C <sub>o(er)</sub>	Effective output capacitance, energy related <sup>I</sup>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0 to 480V, f=1MHz		19		pF	
C <sub>o(tr)</sub>	Effective output capacitance, time related <sup>J</sup>				31		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz		3.5		pF	
R <sub>g</sub>	Gate resistance	f=1MHz		5.7		Ω	
<b>SWITCHING PARAMETERS</b>							
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =480V, I <sub>D</sub> =4A		9	15	nC	
Q <sub>gs</sub>	Gate Source Charge			3.5			nC
Q <sub>gd</sub>	Gate Drain Charge			2.4			nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =300V, I <sub>D</sub> =4A, R <sub>G</sub> =25Ω		20		ns	
t <sub>r</sub>	Turn-On Rise Time			27		ns	
t <sub>D(off)</sub>	Turn-Off DelayTime			25		ns	
t <sub>f</sub>	Turn-Off Fall Time			17		ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =4A, di/dt=100A/μs, V <sub>DS</sub> =100V		384		ns	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =4A, di/dt=100A/μs, V <sub>DS</sub> =100V		3.9		μC	

A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

H. L=60mH, I<sub>AS</sub>=2.2A, V<sub>DD</sub>=150V, R<sub>G</sub>=10Ω, Starting T<sub>J</sub>=25°C.

I. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

J. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

K. L=1.0mH, V<sub>DD</sub>=150V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

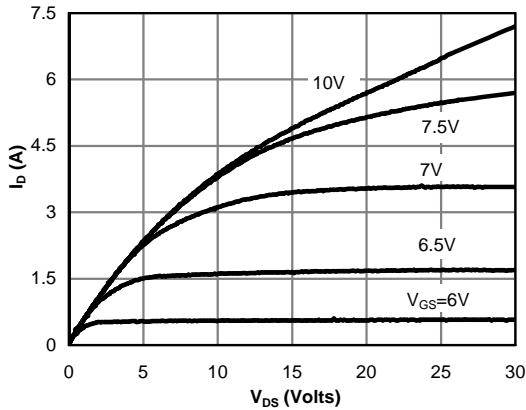


Fig 1: On-Region Characteristics

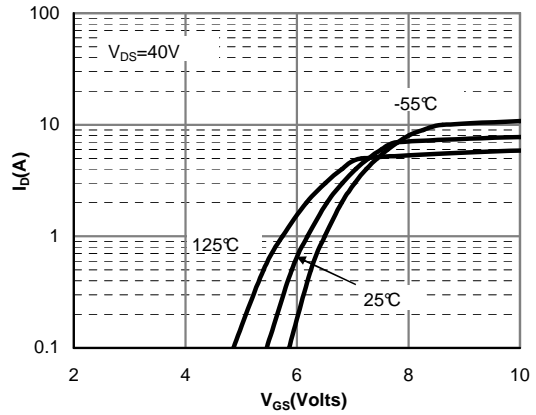


Figure 2: Transfer Characteristics

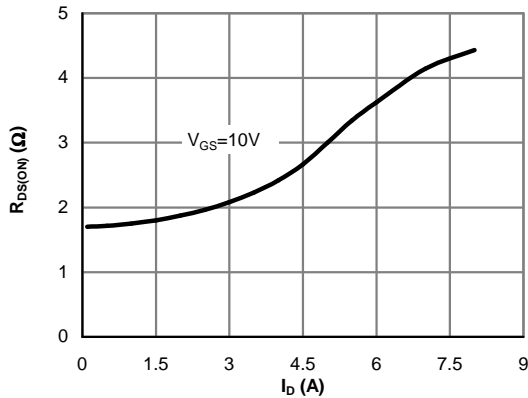


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

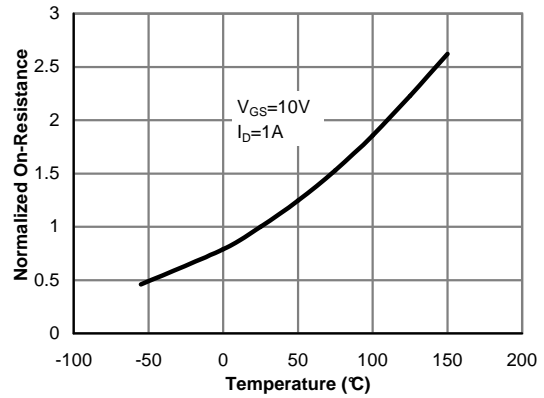


Figure 4: On-Resistance vs. Junction Temperature

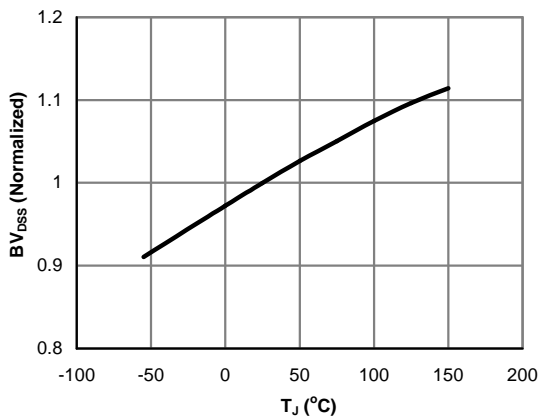


Figure 5: Break Down vs. Junction Temperature

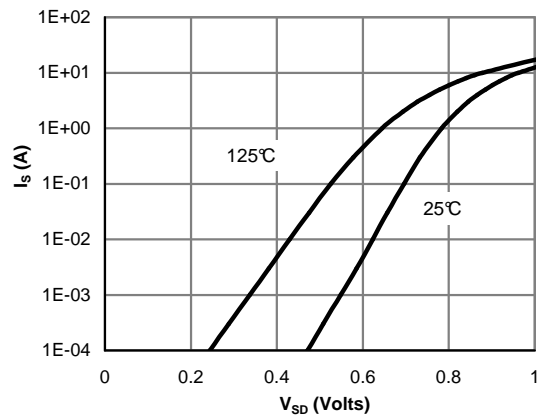


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

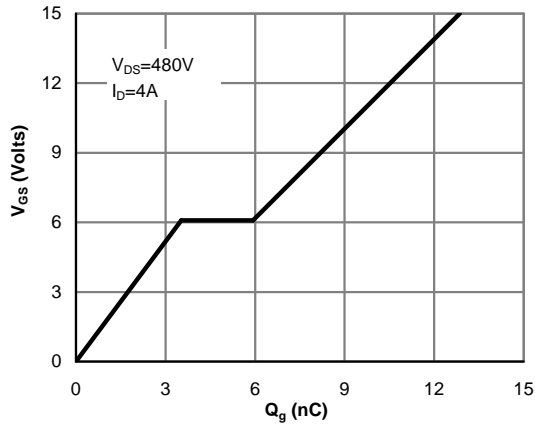


Figure 7: Gate-Charge Characteristics

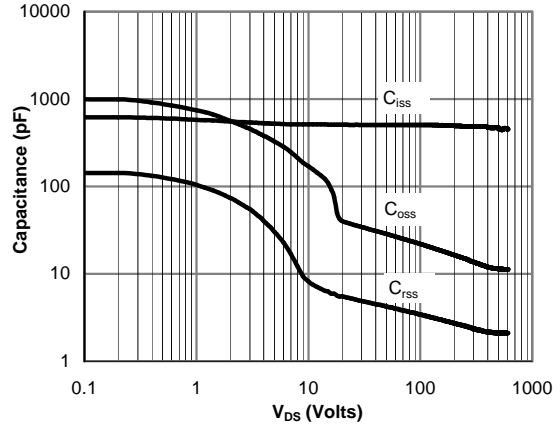


Figure 8: Capacitance Characteristics

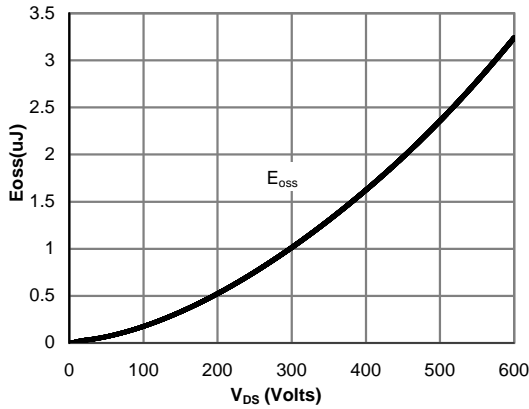


Figure 9: Coss stored Energy

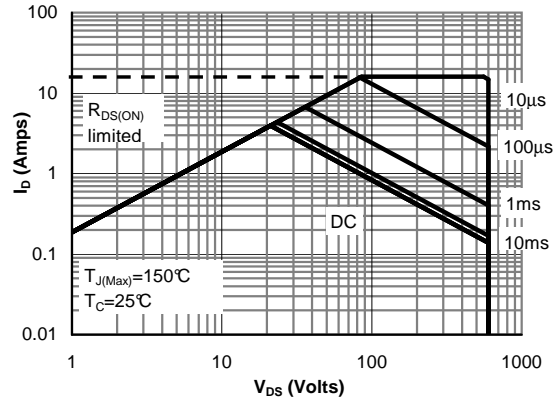


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

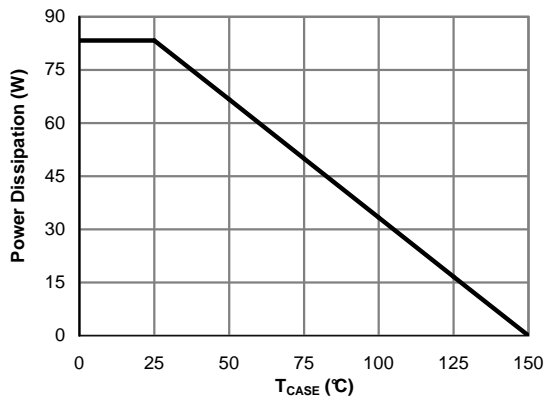


Figure 11: Power De-rating (Note B)

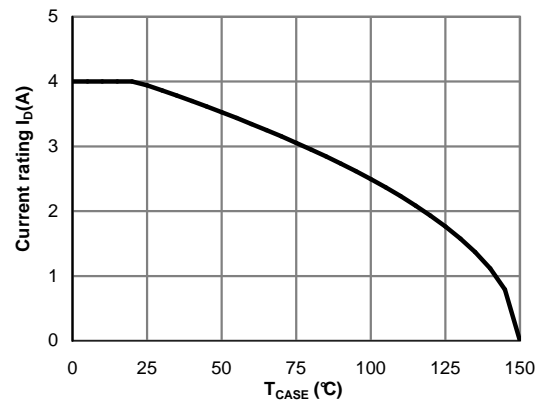


Figure 12: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

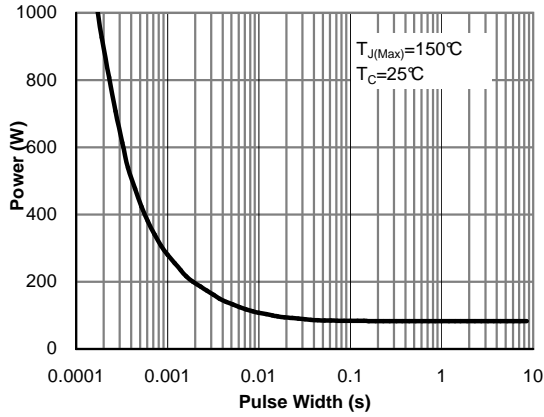


Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)

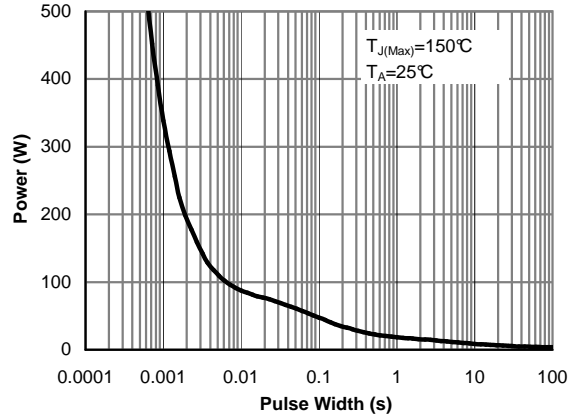


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

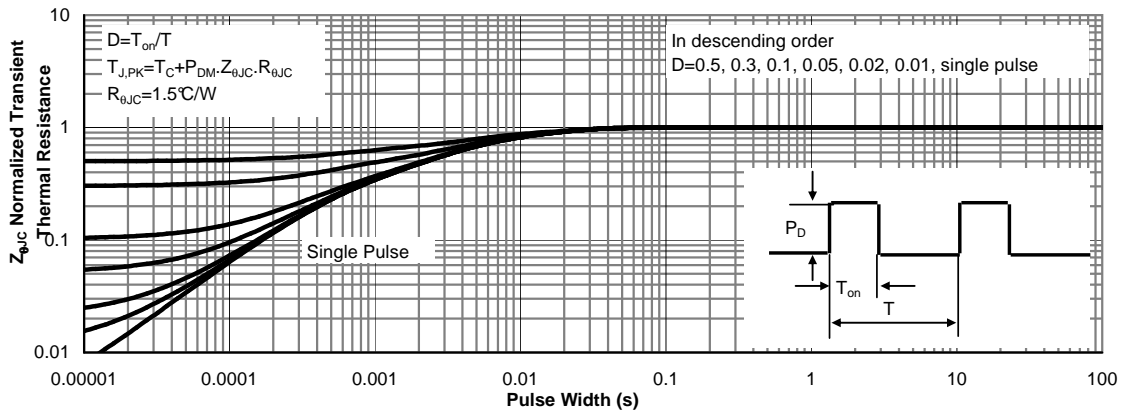


Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

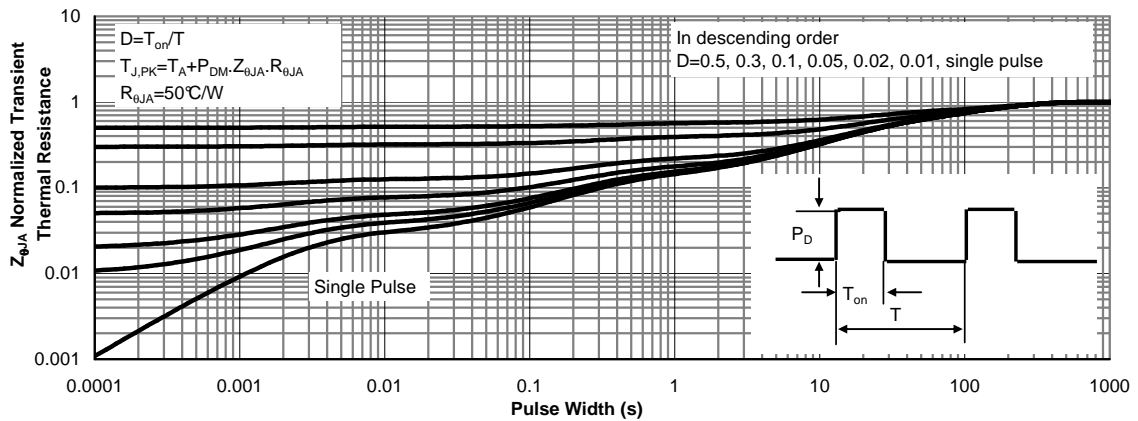
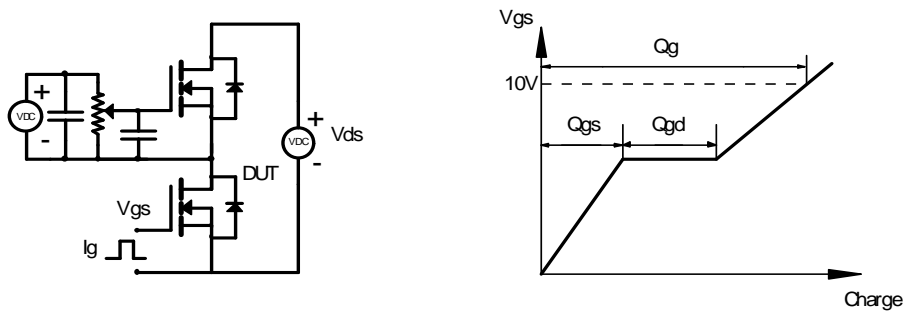
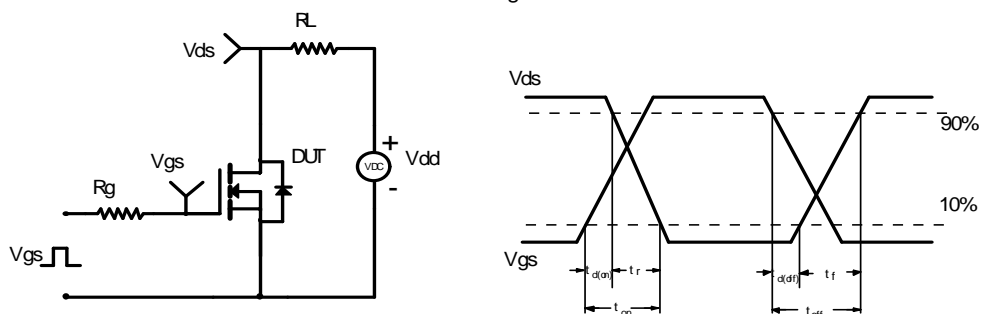


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

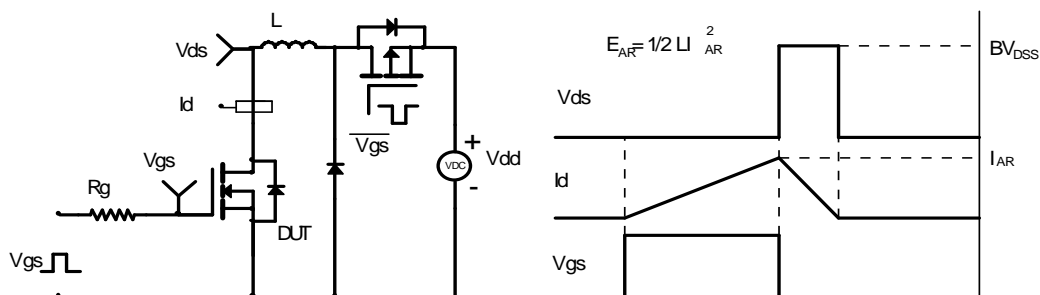
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

