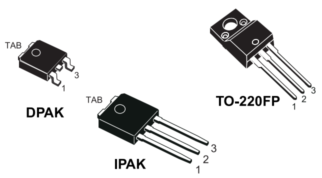
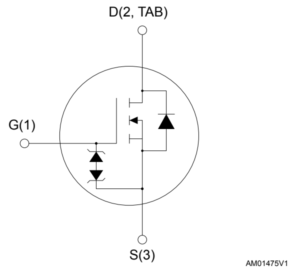
STD2N62K3, STF2N62K3, STU2N62K3

Datasheet

N-channel 620 V, 2.9 Ω typ., 2.2 A K3 Power MOSFETs in DPAK, TO-220FP and IPAK packages





Features

Order code	V_{DS}	$R_{DS(on)}$max.	I_D	Package
STD2N62K3	620 V	3.6 Ω	2.2 A	DPAK
STF2N62K3				TO-220FP
STU2N62K3				IPAK

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These K3 Power MOSFETs are the result of improvements applied to technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Product status link
STD2N62K3
STF2N62K3
STU2N62K3

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
V_{DS}	Drain-source voltage	620			V
V_{GS}	Gate-source voltage	±30			V
I_D	Drain current (continuous) at T_C = 25 °C	2.2	2.2 (1)	2.2	A
I_D	Drain current (continuous) at T_C = 100 °C	1	1 (1)	1	A
I_{DM} (2)	Drain current (pulsed)	8.8			A
P_{TOT}	Total dissipation at T_C = 25 °C	45	20	45	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)	-	2500	-	V
dv/dt (3)	Peak diode recovery voltage slope	12			V/ns
T_j	Operating junction temperature range	-55 to 150			°C
T_{stg}	Storage temperature range				

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 2.2 A, di/dt ≤ 400 A/μs, V_{DSpeak} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.78	6.25	2.78	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	100	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50			°C/W

1. *When mounted on 1inch² FR-4 board, 2 oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not-repetitive	2.2	A
E_{AS} (2)	Single pulse avalanche energy	85	mJ

1. *Pulse width limited by T_j max.*
2. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. **On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	620			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 620 V			1	µA
		V_{GS} = 0 V, V_{DS} = 620 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.1 A		2.9	3.6	Ω

1. *Defined by design, not subject to production test.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	340	-	pF
C_{oss}	Output capacitance			26		
C_{rss}	Reverse transfer capacitance			4		
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 496 V, V_{GS} = 0 V	-	17	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 2.2 A, V_{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	15	-	nC
Q_{gs}	Gate-source charge			3		
Q_{gd}	Gate-drain charge			9		

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 310 V, I_D = 1.1 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	8	-	ns
t_r	Rise time			4.4		
$t_{d(off)}$	Turn-off delay time			21		
t_f	Fall time			22		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.2	A
I_{SDM} (1)	Source-drain current (pulsed)				8.8	
V_{SD} (2)	Forward on voltage	I_{SD} = 2.2 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2.2 A, di/dt = 100 A/µs V_{DD} = 60 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	200		ns
Q_{rr}	Reverse recovery charge			0.9		µC
I_{RRM}	Reverse recovery current			9		A
t_{rr}	Reverse recovery time	I_{SD} = 2.2 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C(see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	240		ns
Q_{rr}	Reverse recovery charge			1.15		µC
I_{RRM}	Reverse recovery current			10		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{gs} = ±1 mA, I_D = 0 A	±30			V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for DPAK and IPAK

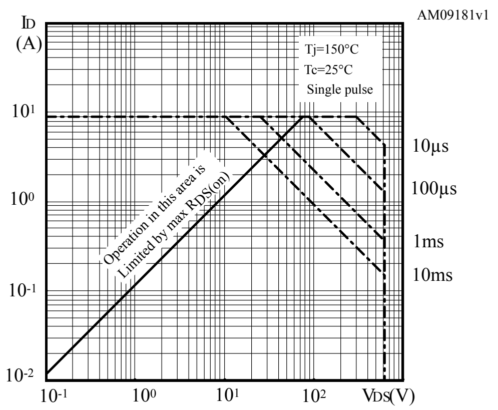


Figure 2. Thermal impedance for DPAK and IPAK

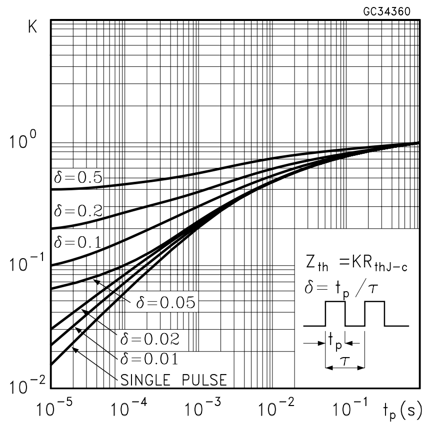


Figure 3. Safe operating area for TO-220FP

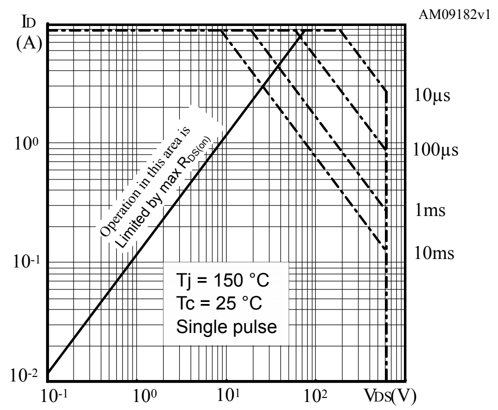


Figure 4. Thermal impedance for TO-220FP

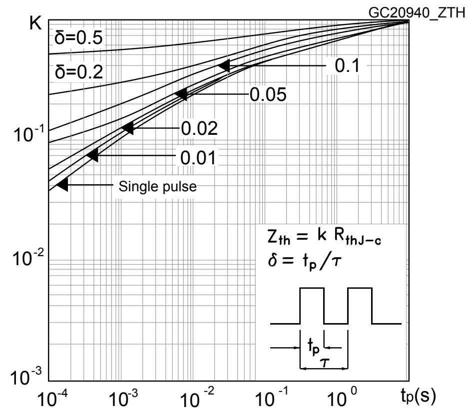


Figure 5. Output characterisics

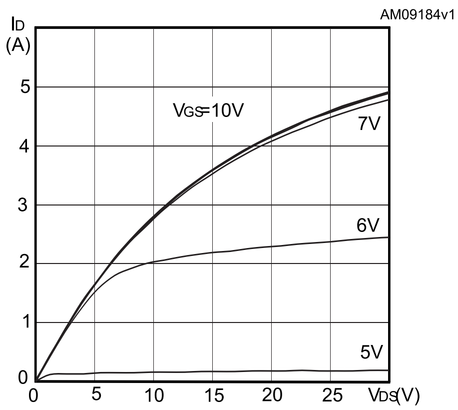


Figure 6. Transfer characteristics

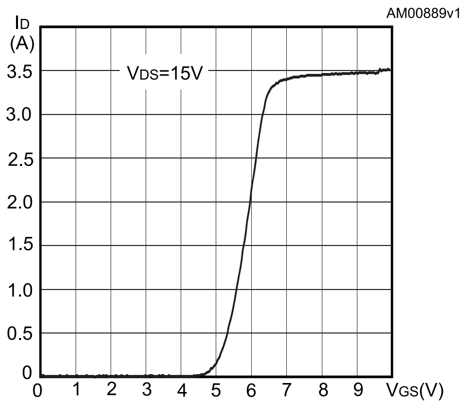


Figure 7. Gate charge vs gate-source voltage

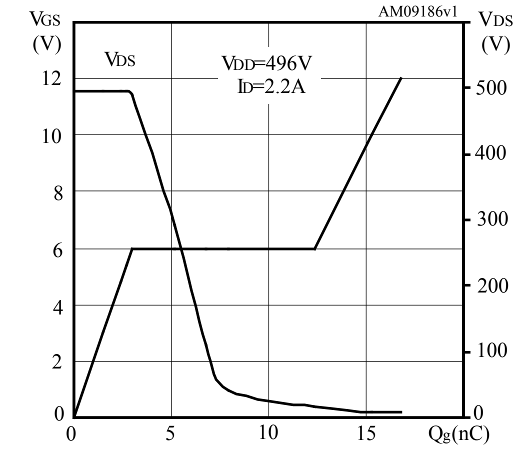


Figure 8. Static drain-source on-resistance

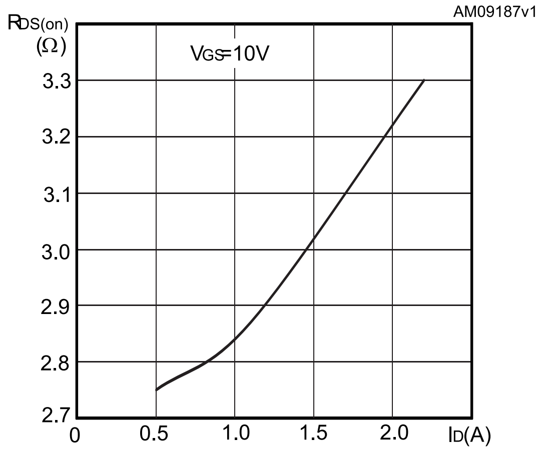


Figure 9. Capacitance variations

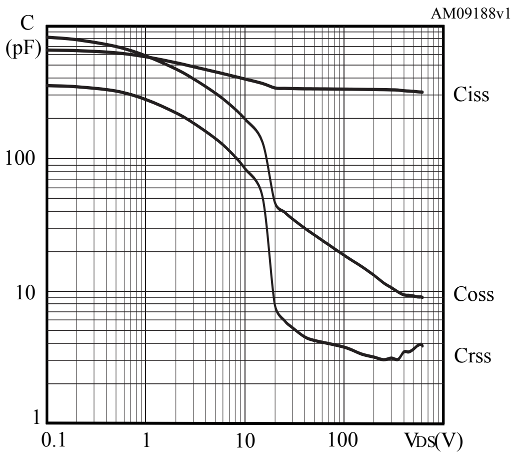


Figure 10. Output capacitance stored energy

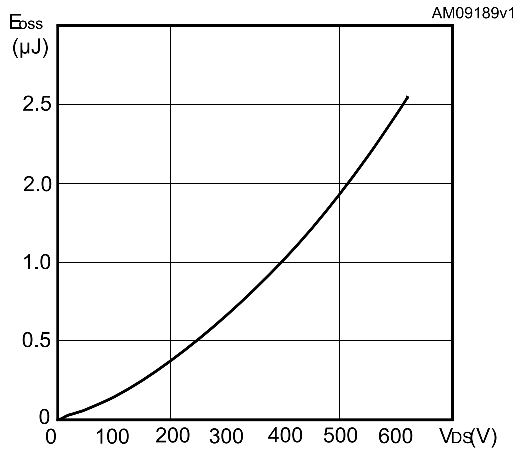


Figure 11. Normalized gate threshold voltage vs temperature

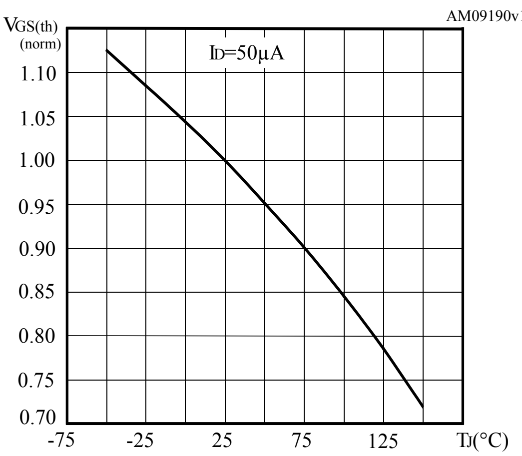


Figure 12. Normalized on-resistance vs temperature

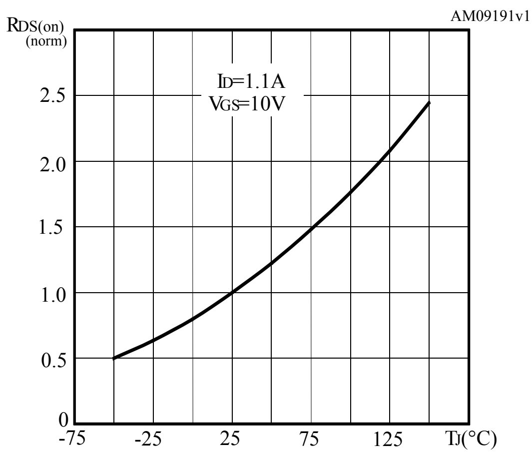


Figure 13. Source-drain diode forward characteristics

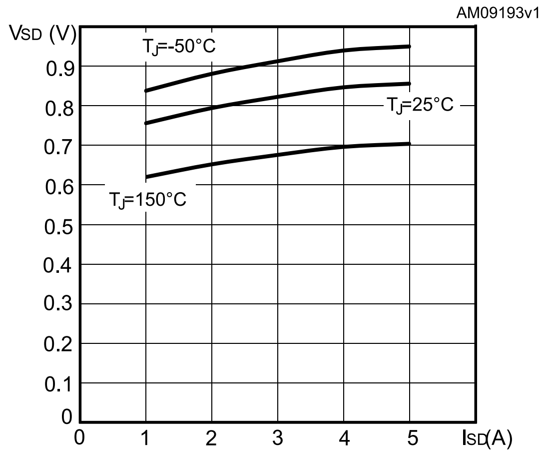


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

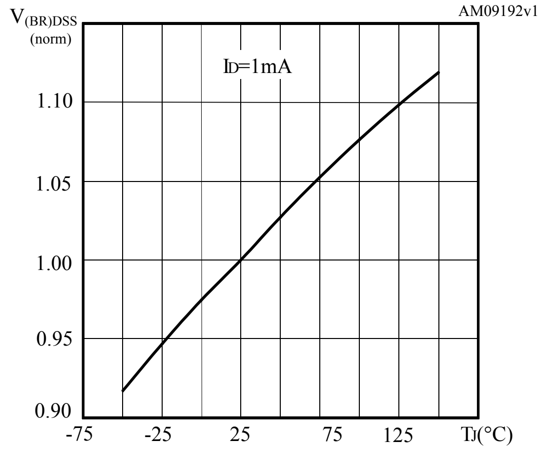
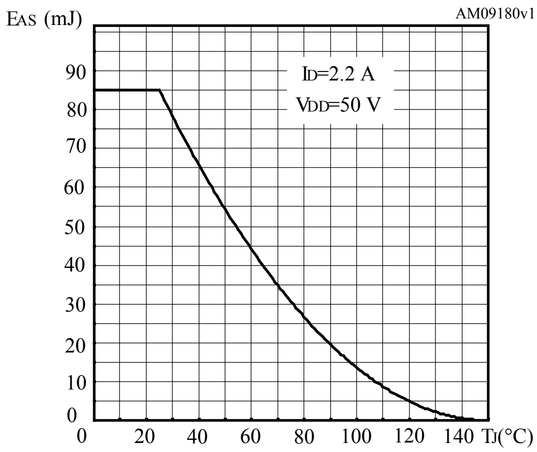


Figure 15. Maximum avalanche energy vs starting T_j



3 Test circuits

Figure 16. Test circuit for resistive load switching times

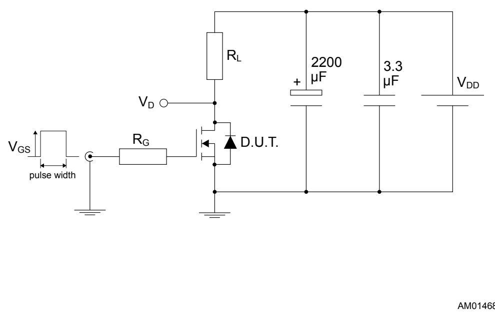


Figure 17. Test circuit for gate charge behavior

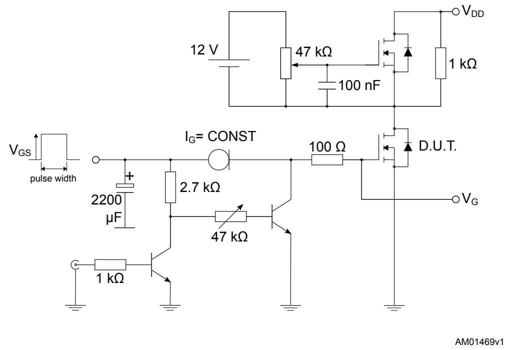


Figure 18. Test circuit for inductive load switching and diode recovery times

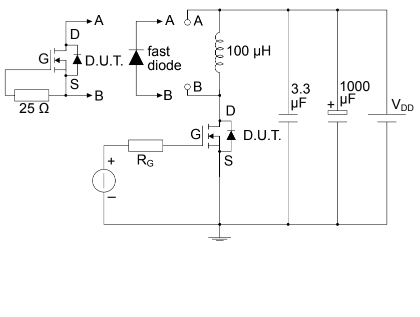


Figure 19. Unclamped inductive load test circuit

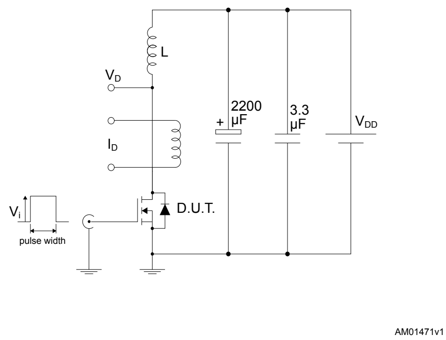


Figure 20. Unclamped inductive waveform

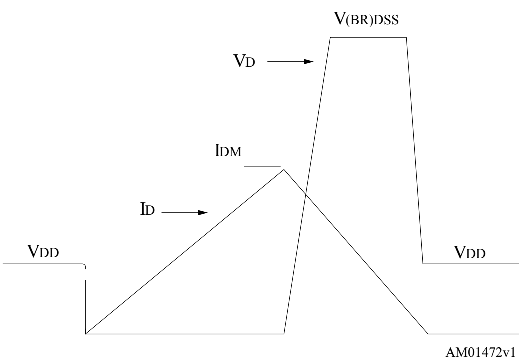


Figure 21. Switching time waveform