STB70N10F4, STD70N10F4
STP70N10F4, STW70N10F4

N-channel 100 V, 0.015 Ω, 60 A, Power MOSFET in TO-220, DPAK, TO-247, D²PAK

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STB70N10F4	100 V	< 0.0195 Ω	65 A
STD70N10F4	100 V	< 0.0195 Ω	60 A
STP70N10F4	100 V	< 0.0195 Ω	65 A
STW70N10F4	100 V	< 0.0195 Ω	65 A

- Exceptional dv/dt capability
- Extremely low on-resistance $R_{DS(on)}$
- 100% avalanche tested

Application

- Switching applications

Description

This Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performance.

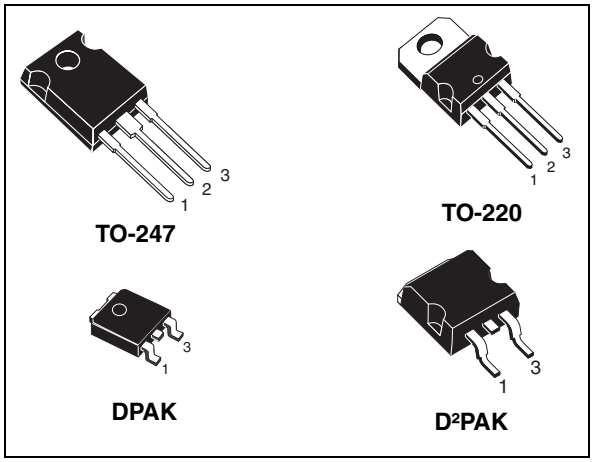

Figure 1. Internal schematic diagram

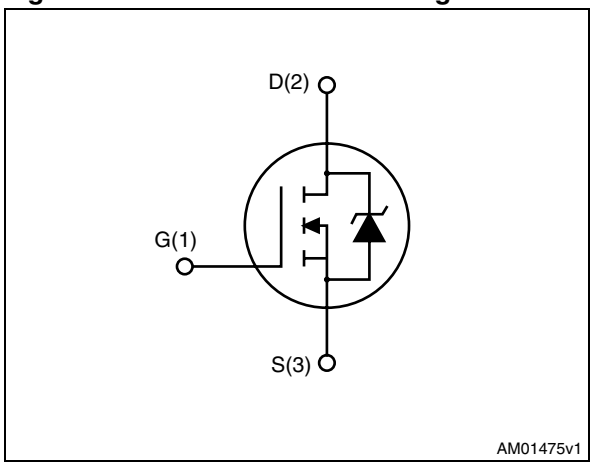

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB70N10F4	70N10F4	D²PAK	Tape and reel
STD70N10F4	70N10F4	DPAK	Tape and reel
STP70N10F4	70N10F4	TO-220	Tube
STW70N10F4	70N10F4	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247, D²PAK	DPAK	
V_{DS}	Drain-source voltage (V_{GS} = 0)	100		V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (continuous) at T_C = 25 °C	65	60	A
I_D	Drain current (continuous) at T_C = 100 °C	46	43	A
I_{DM} (1)	Drain current (pulsed)	260	240	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	125	W
	Derating factor	1	0.83	W/°C
E_{AS} (2)	Single pulse avalanche energy	120		mJ
T_{stg}	Storage temperature	– 55 to 175		°C
T_j	Max. operating junction temperature			

1. Pulse width limited by safe operating area
2. Starting T_j = 25 °C, I_D= 32.5 A, V_{DD}= 45 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220, TO-247, D²PAK	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	1.2	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	50 (1)	°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on FR-4 board of 1 inch², 2 oz Cu

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating,T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 30 A		0.015	0.0195	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	5800	-	pF
C_{oss}	Output capacitance			300		pF
C_{rss}	Reverse transfer capacitance			190		pF
Q_g	Total gate charge	V_{DD} = 80 V, I_D = 65 A, V_{GS} = 10 V *(see Figure 16)*	-	85	-	nC
Q_{gs}	Gate-source charge			20		nC
Q_{gd}	Gate-drain charge			25		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 50 V, I_D = 30 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 15)*	-	30 20	-	ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	V_{DD} = 50 V, I_D = 30 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 15)*	-	65 20	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		60	A
I_{SDM} (1)	Source-drain current (pulsed)				240	A
V_{SD} (2)	Forward on voltage	I_{SD} = 60 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 60 A, V_{DD} = 25 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 17)*	-	80		ns
Q_{rr}	Reverse recovery charge			280		nC
I_{RRM}	Reverse recovery current			6.7		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, TO-247, D²PAK

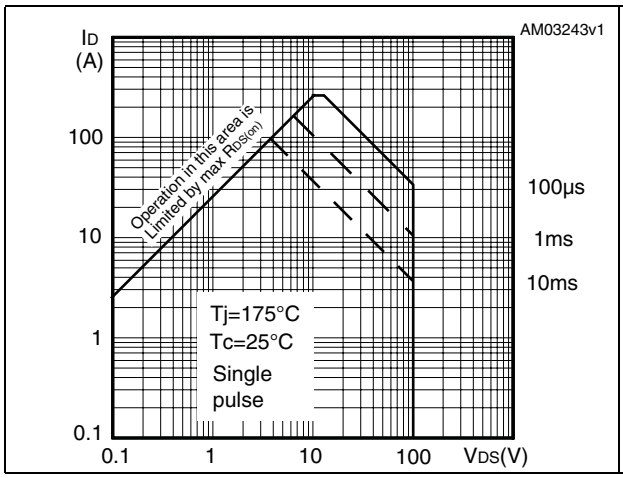

Figure 3. Thermal impedance for TO-220, TO-247, D²PAK

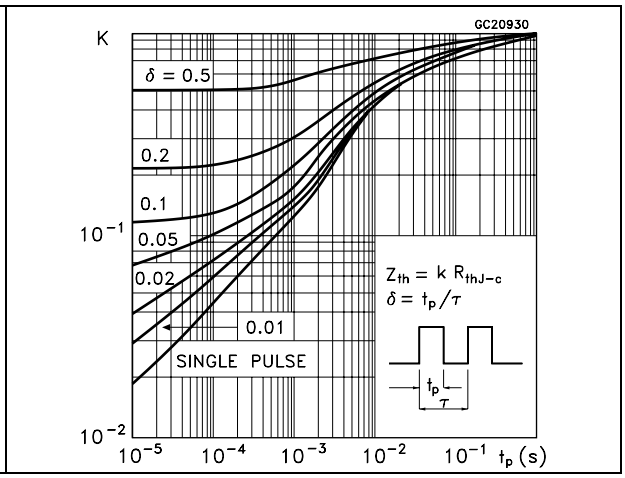

Figure 4. Safe operating area for DPAK

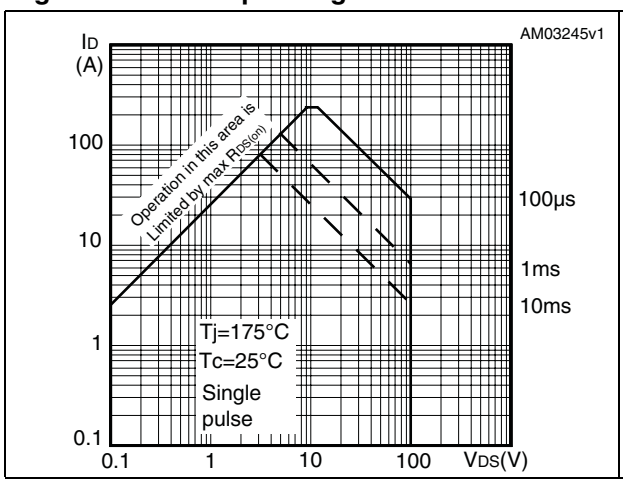

Figure 5. Thermal impedance for DPAK

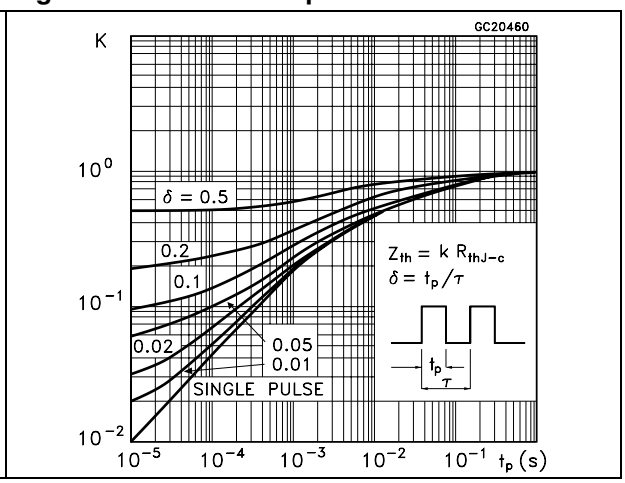

Figure 6. Output characteristics

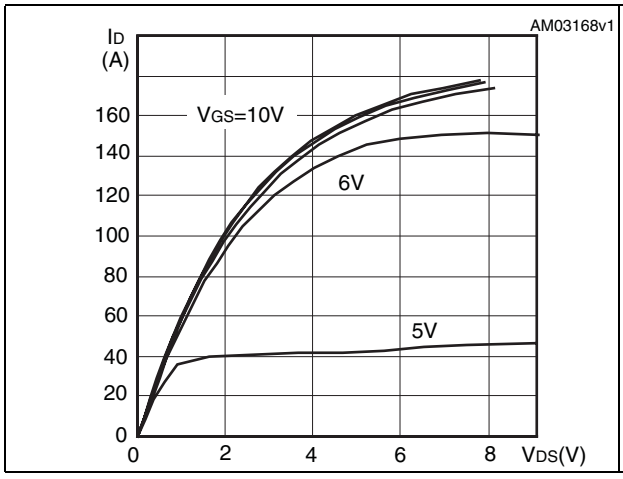

Figure 7. Transfer characteristics

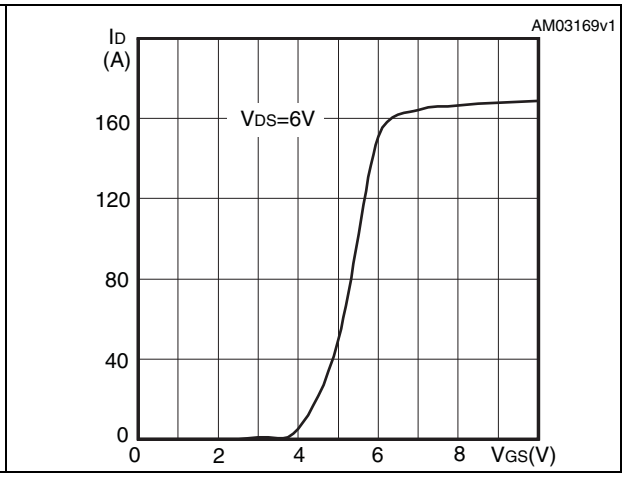

Figure 8. Normalized B_{VDSS} vs temperature

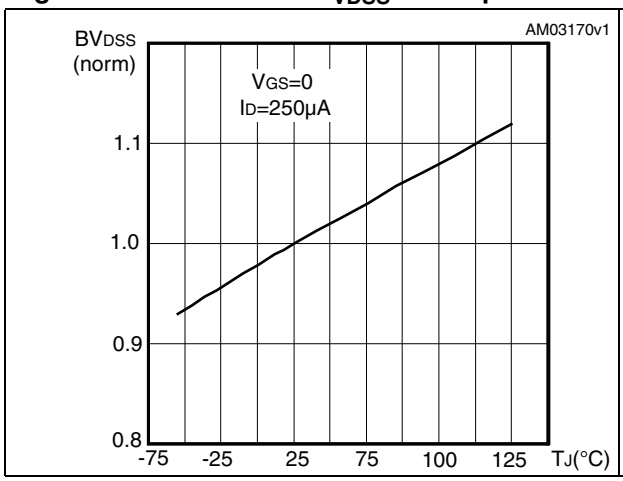

Figure 9. Static drain-source on resistance

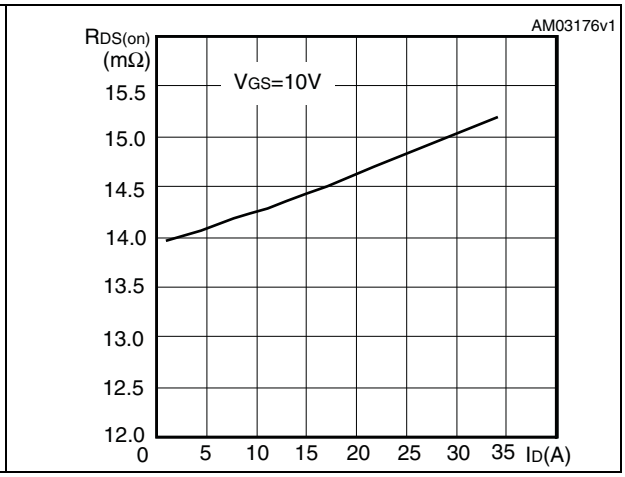

Figure 10. Gate charge vs gate-source voltage

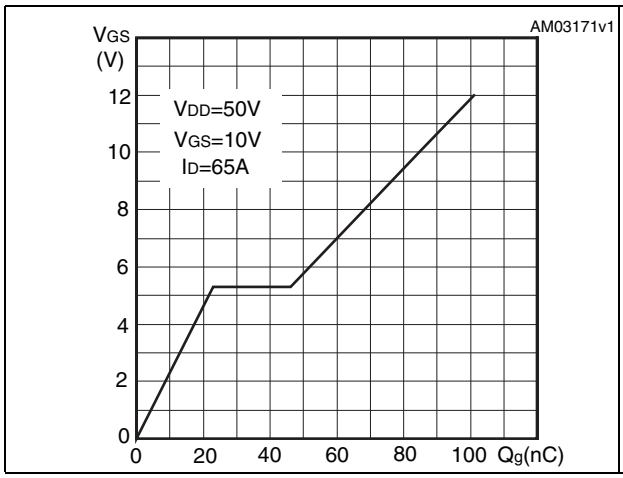

Figure 11. Capacitance variations

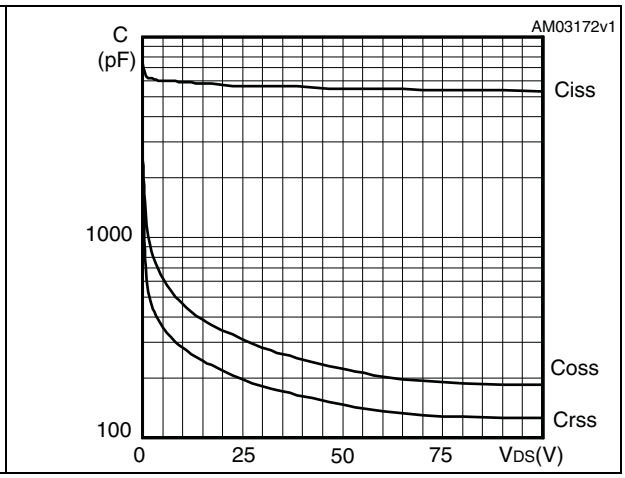

Figure 12. Normalized gate threshold voltage vs temperature

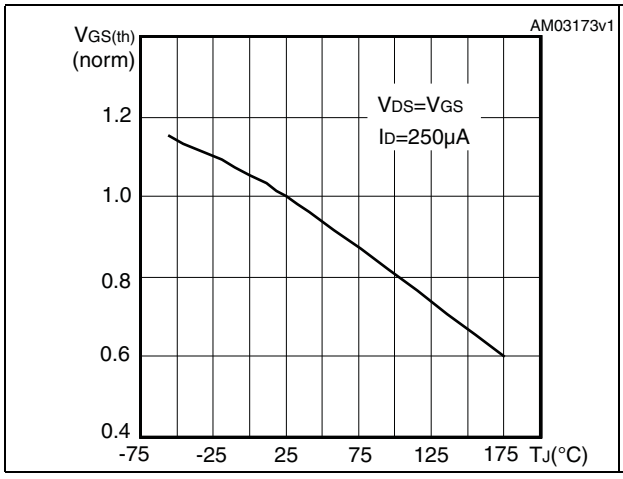

Figure 13. Normalized on resistance vs temperature

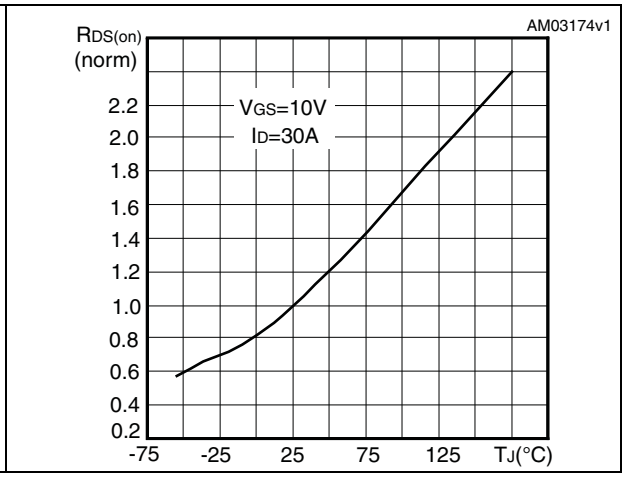

Figure 14. Source-drain diode forward characteristics