STD80N10F7, STF80N10F7, STH80N10F7-2, STP80N10F7

N-channel 100 V, 0.008 Ω typ., 80 A Power MOSFETs in DPAK, TO-220FP, H²PAK-2 and TO-220

Datasheet - production data

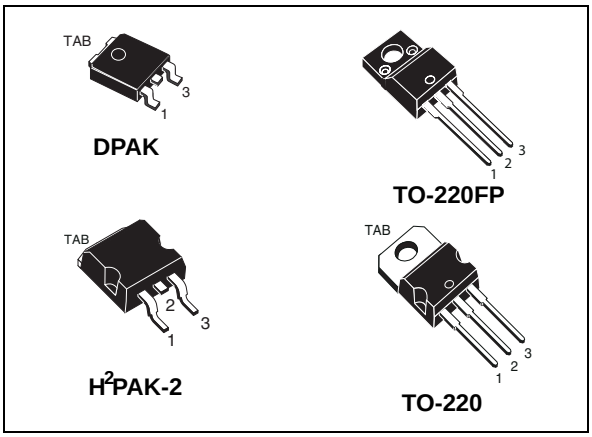
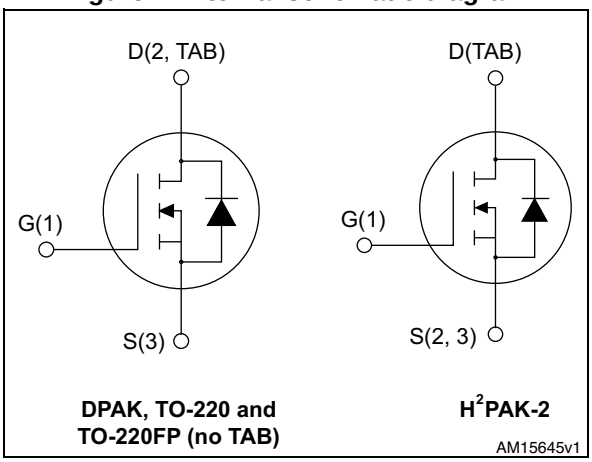


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D	P_{TOT}
STD80N10F7	100 V	0.01 Ω	70 A	85 W
STF80N10F7		0.01 Ω	40 A	30 W
STH80N10F7-2		0.0095 Ω	80 A	110 W
STP80N10F7		0.01 Ω		

- Extremely low gate charge
- Ultra low on-resistance
- Low gate input resistance

Applications

- Switching applications

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD80N10F7	80N10F7	DPAK	Tape and reel
STF80N10F7		TO-220FP	Tube
STH80N10F7-2		H²PAK-2	Tape and reel
STP80N10F7		TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	H^2PAK-2 TO-220	TO-220FP	
V_{DS}	Drain-source voltage	100			V
V_{GS}	Gate-source voltage	± 20			V
I_D	Drain current (continuous) at T_C = 25 °C	70	80	40	A
I_D	Drain current (continuous) at T_C = 100 °C	48	54	30	A
I_{DM} (1)	Drain current (pulsed)	280	320	160	A
P_{TOT}	Total dissipation at T_C = 25 °C	85	110	30	W
T_{stg}	Storage temperature	- 55 to 175			°C
T_j	Max. operating junction temperature				

1. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	H^2PAK-2	TO-220	
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max	50		35		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		62.5		62.5	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.76	5	1.36		°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V V_{DS} = 100 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = 20 V			100	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	for DPAK, TO-220 and TO-220FP: I_D = 40 A, V_{GS}=10 V		0.0085	0.010	Ω
		for H^2PAK-2: V_{GS}=10 V, I_D=40 A		0.008	0.0095	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	3100	-	pF
C_{oss}	Output capacitance		-	700	-	pF
C_{rss}	Reverse transfer capacitance		-	45	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10 V (see *Figure 18*)	-	45	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	13	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_d(on)	Turn-on delay time	V_{DD} = 50 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19* and *Figure 22*)	-	19	-	ns
t_r	Rise time		-	32	-	ns
t_d(off)	Turn-off delay time		-	36	-	ns
t_f	Fall time		-	13	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM} (1)	Source-drain current (pulsed)		-		320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A, di/dt = 100 A/µs V_{DD} = 80 V, T_j=150 °C (see *Figure 22*)	-	70		ns
Q_{rr}	Reverse recovery charge		-	125		nC
I_{RRM}	Reverse recovery current		-	3.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK, H²PAK-2 and TO-220

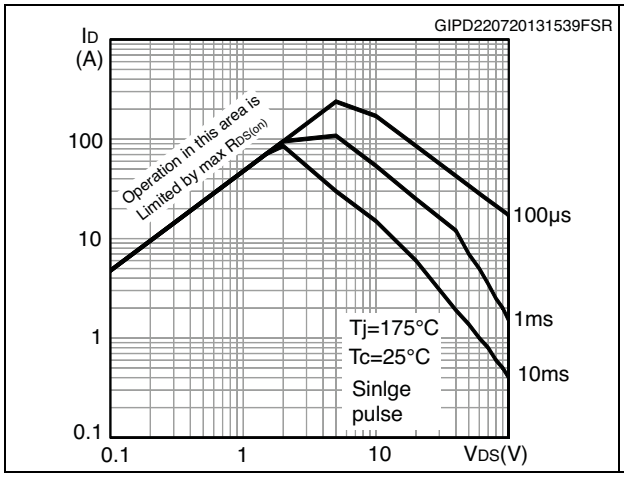


Figure 3. Thermal impedance for DPAK, H²PAK-2 and TO-220

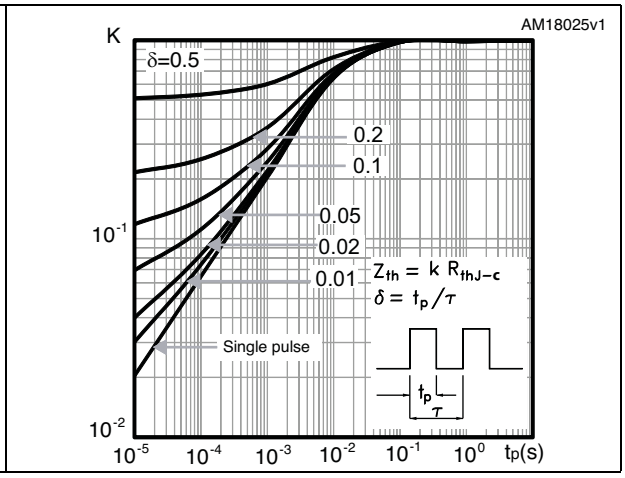


Figure 4. Safe operating area for TO-220FP

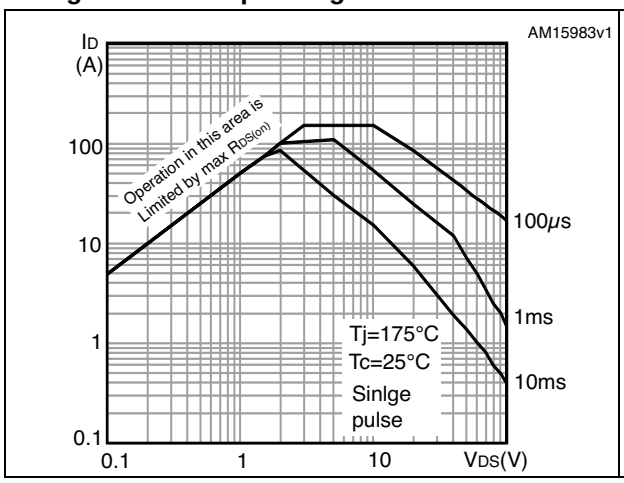


Figure 5. Thermal impedance for TO-220FP

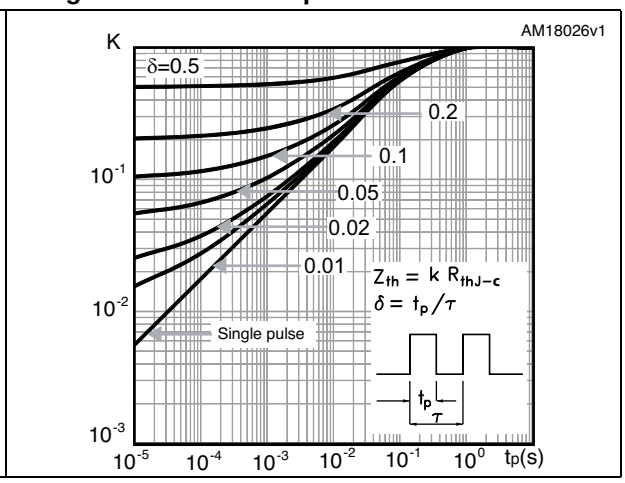


Figure 6. Output characteristics

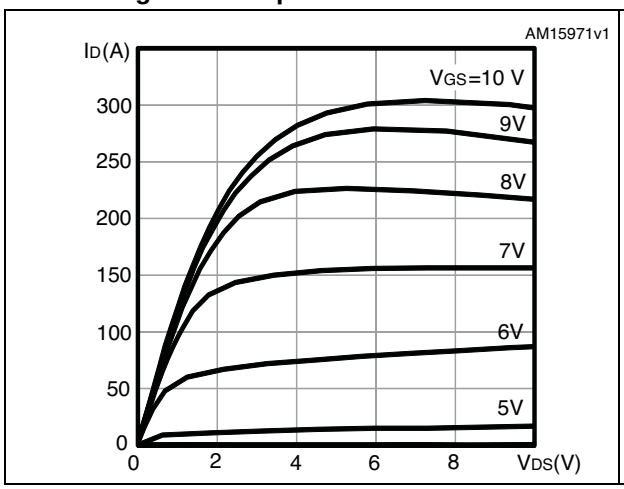


Figure 7. Transfer characteristics

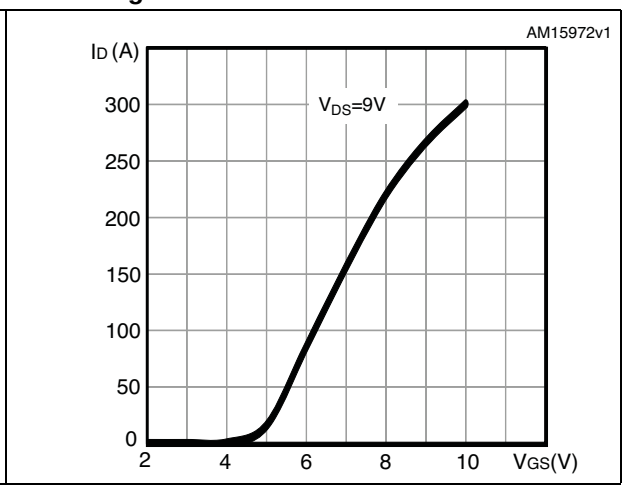


Figure 8. Static drain-source on-resistance for DPAK and TO-220

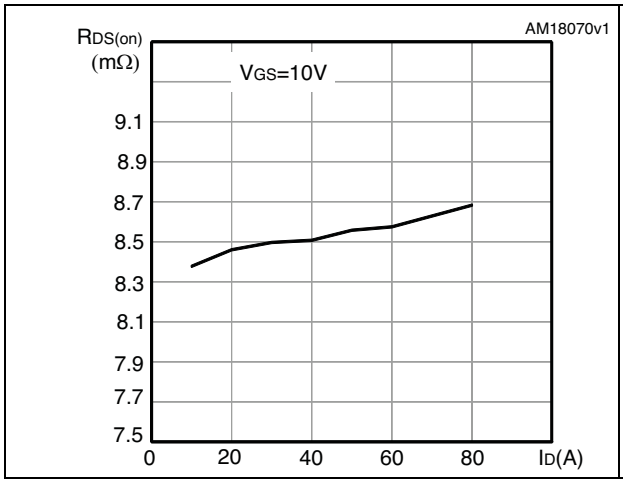


Figure 9. Static drain-source on-resistance for H^2PAK-2

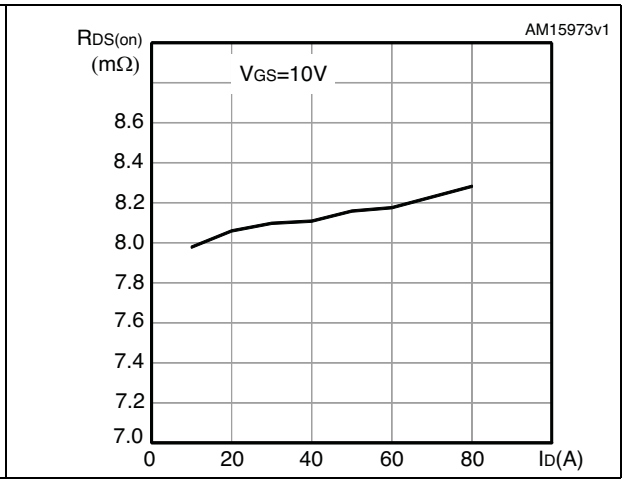


Figure 10. Static drain-source on-resistance for TO-220FP

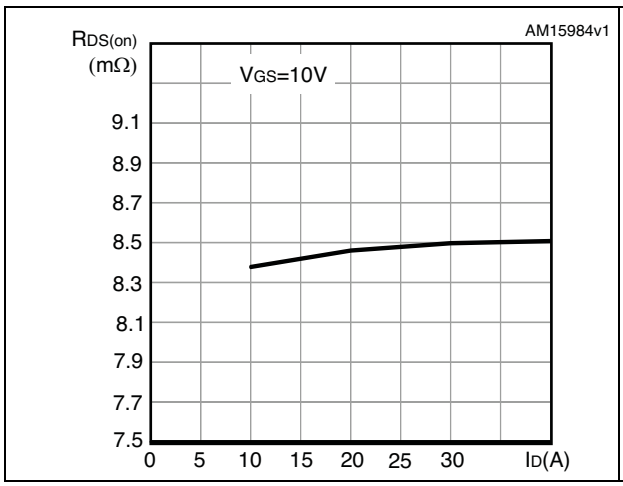


Figure 11. Gate charge vs gate-source voltage

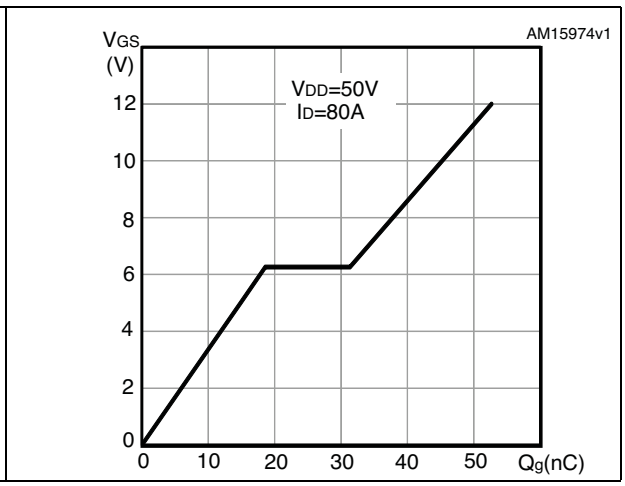


Figure 12. Capacitance variations

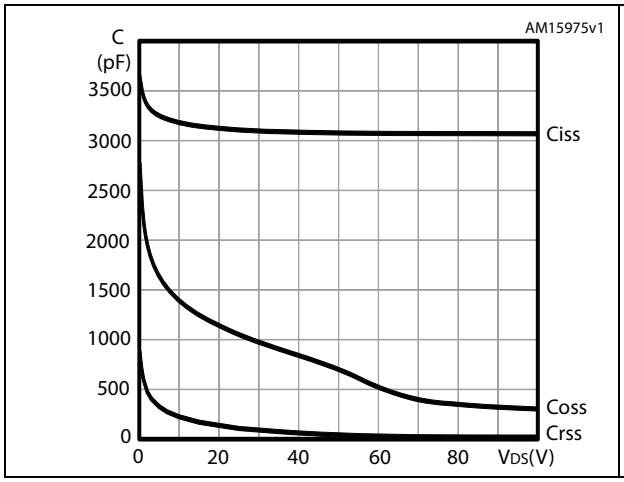


Figure 13. Normalized gate threshold voltage vs temperature

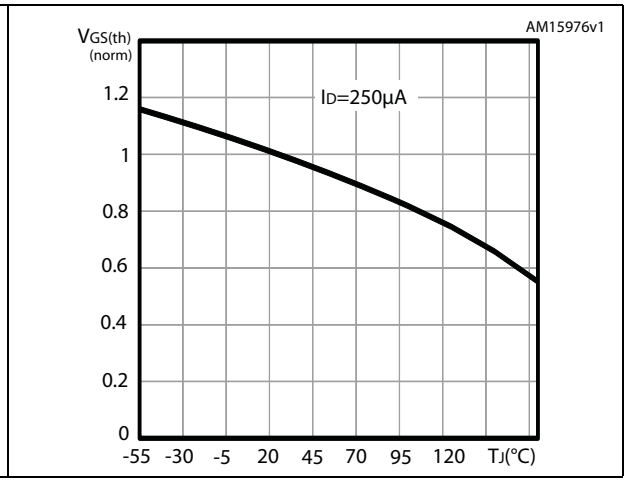


Figure 14. Normalized on-resistance vs temperature

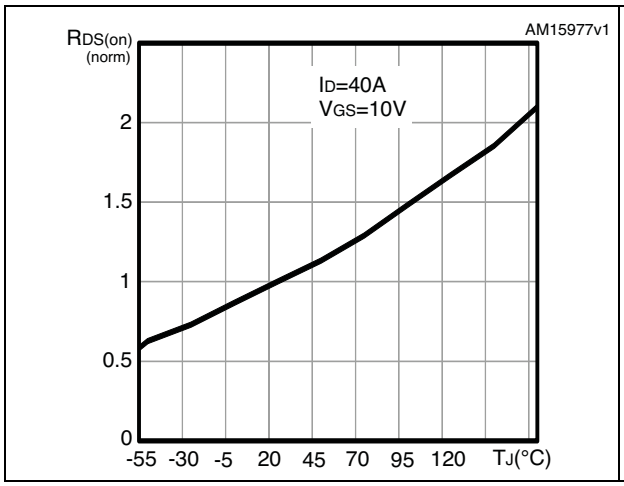


Figure 15. Source-drain diode forward characteristics

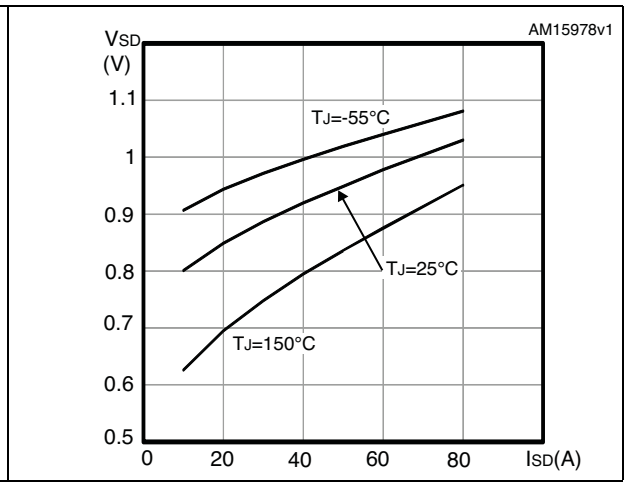
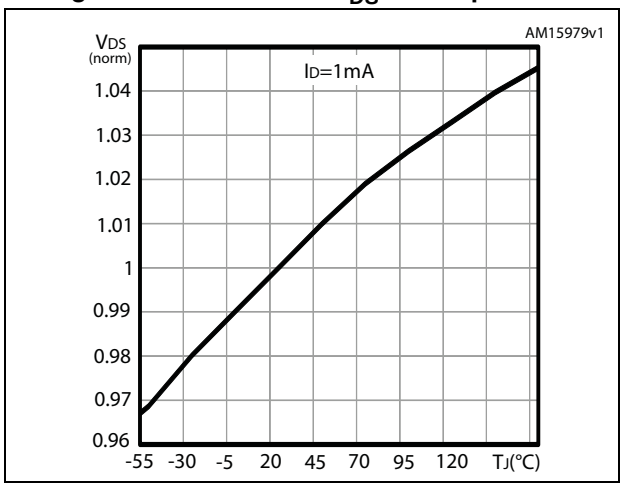


Figure 16. Normalized V_{DS} vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load

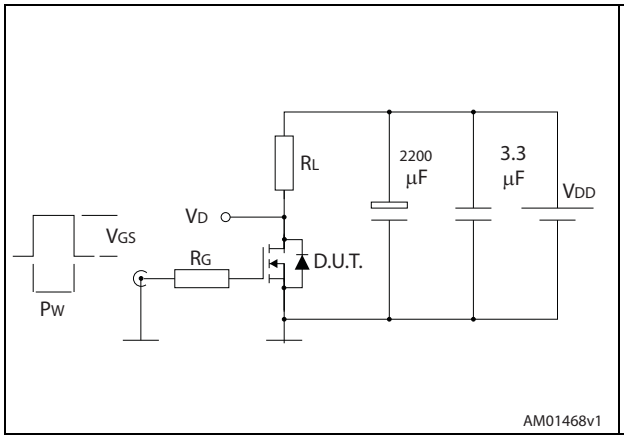


Figure 18. Gate charge test circuit

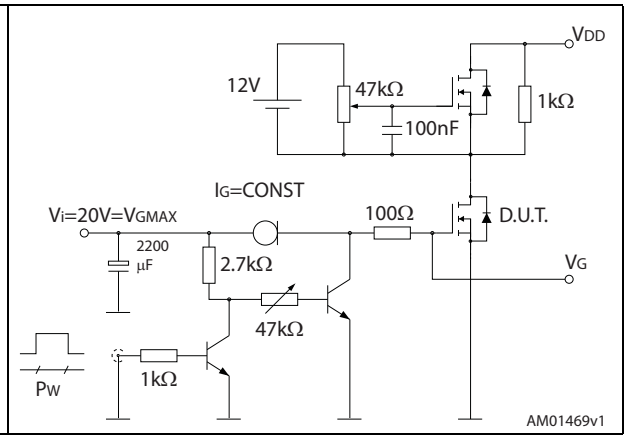


Figure 19. Test circuit for inductive load switching and diode recovery times

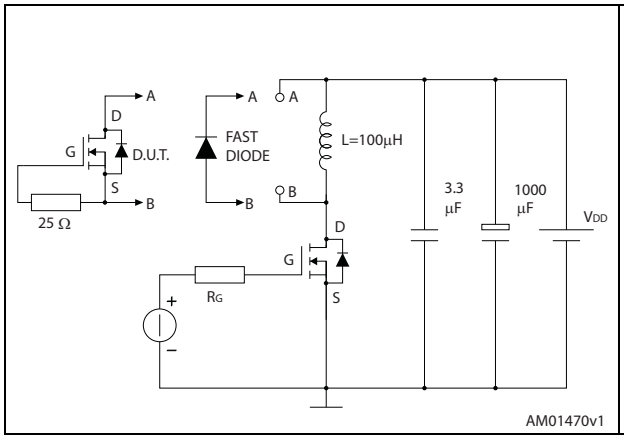


Figure 20. Unclamped inductive load test circuit

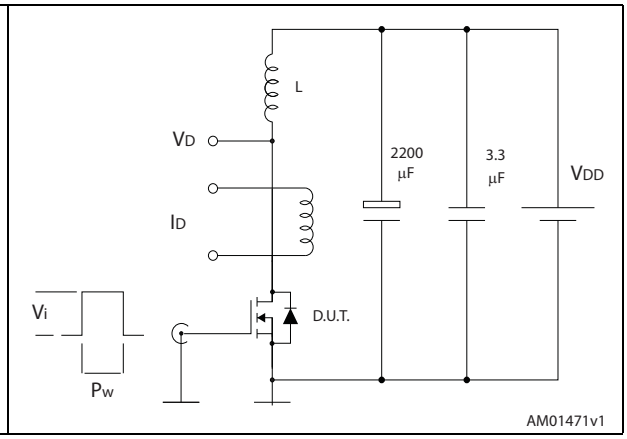


Figure 21. Unclamped inductive waveform

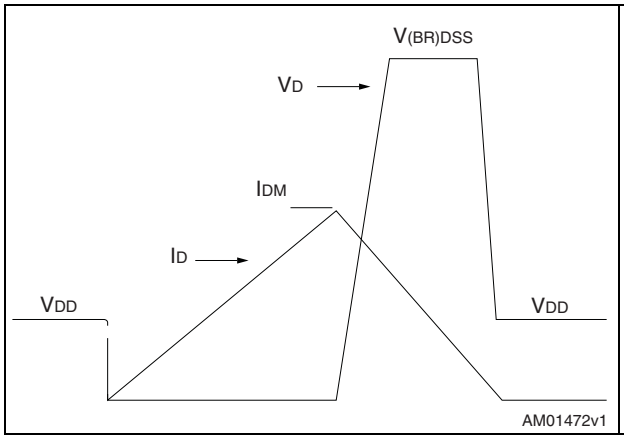


Figure 22. Switching time waveform