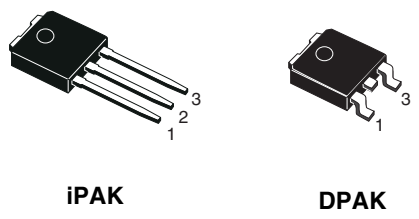
STD16NF06L
STD16NF06L-1

N-channel 60V - 0.060Ω - 24A - DPAK/IPAK
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STD16NF06L-1	60V	<0.070Ω	24A
STD16NF06L	60V	<0.070Ω	24A

- Logic level device
- Low threshold drive



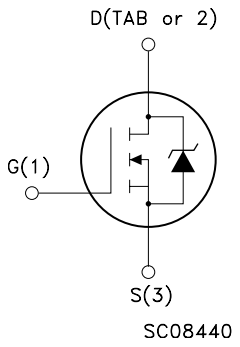
Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD16NF06L-1	D16NF06L	IPAK	Tube
STD16NF06LT4	D16NF06L	DPAK	Tape & reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source voltage	± 18	V
I_D	Drain current (continuous) at T_C = 25°C	24	A
I_D	Drain current (continuous) at T_C = 100°C	17	A
I_{DM}(1)	Drain current (pulsed)	96	A
P_{tot}	Total dissipation at T_C = 25°C	40	W
	Derating Factor	0.27	W/°C
dv/dt(2)	Peak diode recovery avalanche energy	11.5	V/ns
E_{AS} (3)	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 16A$, di/dt $\leq 200A/\mu s$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting T_j = 25 °C, I_D = 20A, V_{DD} = 48V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	3.75	°C/W
Rthj-pcb	Thermal resistance junction-to PCB max	62	°C/W
T_J	Maximum lead temperature for soldering purpose (1)	300	°C

1. When Mounted on 1 inch2 FR-4 board, 2 oz. of Cu.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 18V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 8A V_{GS} = 5V, I_D = 8A		0.060 0.070	0.070 0.085	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 12A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		370 69 30		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 30V, I_D = 8A R_G = 4.7Ω V_{GS} = 5V		12 30 20 6		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 30V, I_D = 8A, V_{GS} = 5V, R_G = 4.7Ω		7.5 2.5 4.2		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				16 64	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 16A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 16A, di/dt = 100A/µs, V_{DD} = 25V, T_j = 150°C		53 85 3.2		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

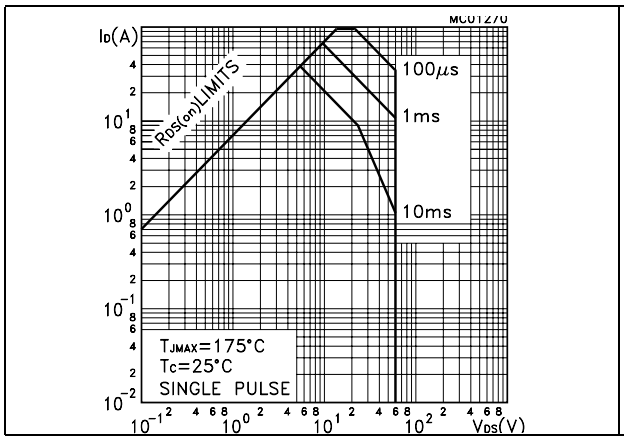


Figure 2. Thermal impedance

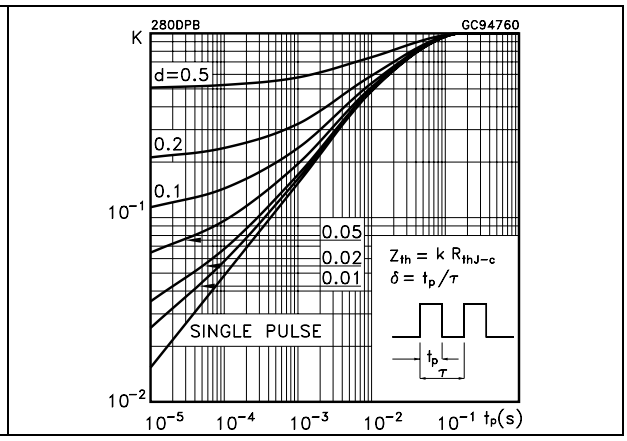


Figure 3. Output characteristics

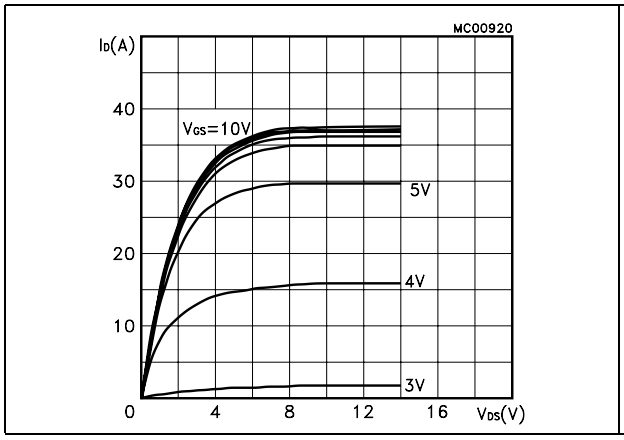


Figure 4. Transfer characteristics

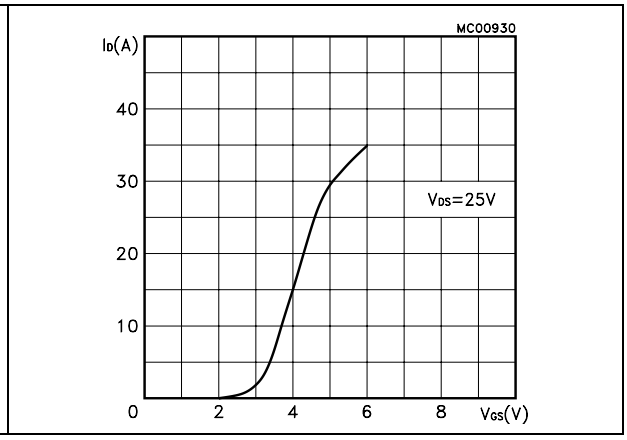


Figure 5. Transconductance

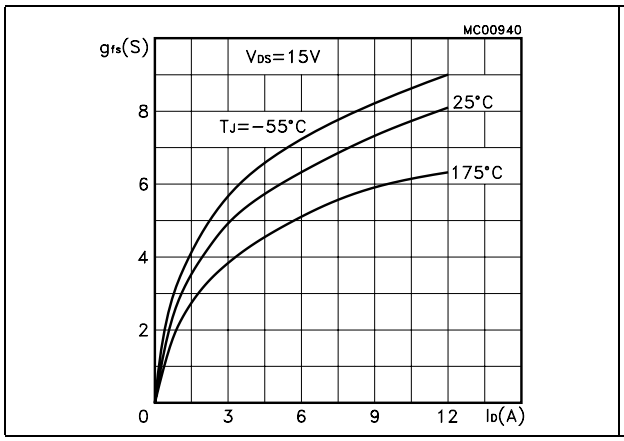


Figure 6. Static drain-source on resistance