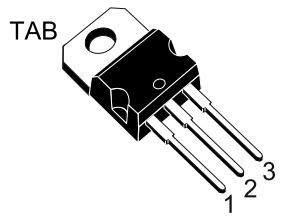
STP130N6F7

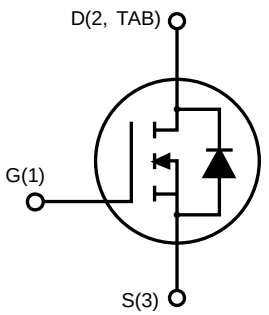
N-channel 60 V, 4.2 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP130N6F7	60 V	5.0 mΩ	80 A	160 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STP130N6F7	130N6F7	TO-220	Tube

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_{case} = 25 °C	80	A
	Drain current (continuous) at T_{case} = 100 °C	80	
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	160	W
E_{AS} (3)	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature	175 to -55	°C
T_j	Operating junction temperature		

Notes:

(1) Current is limited by package.

(2) Pulse width is limited by safe operating area.

(3) starting T_j = 25 °C, I_D = 20 A, V_{DD} = 40 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.94	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A		4.2	5.0	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2600	-	pF
C_{oss}	Output capacitance		-	1200	-	
C_{rss}	Reverse transfer capacitance		-	115	-	
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 80 A, V_{GS} = 10 V	-	42	-	nC
Q_{gs}	Gate-source charge		-	13.6	-	
Q_{gd}	Gate-drain charge		-	13	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see	-	24	-	ns
t_r	Rise time		-	44	-	
$t_{d(off)}$	Turn-off delay time		-	62	-	
t_f	Fall time		-	24	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 80 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A, di/dt = 100 A/µs, V_{DD} = 48 V (see	-	50		ns
Q_{rr}	Reverse recovery charge		-	56		nC
I_{RRM}	Reverse recovery current		-	2.2		A

Notes:

(1) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

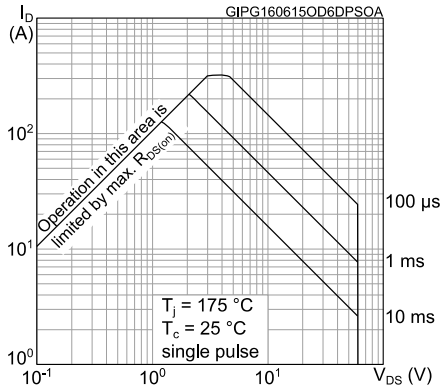


Figure 3: Thermal impedance

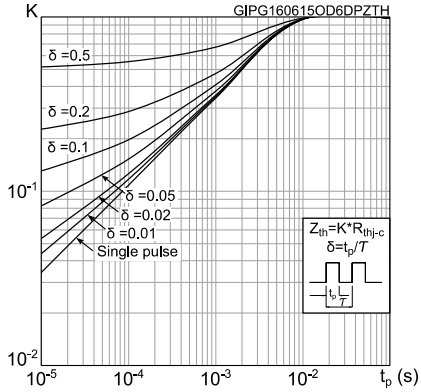


Figure 4: Output characteristics

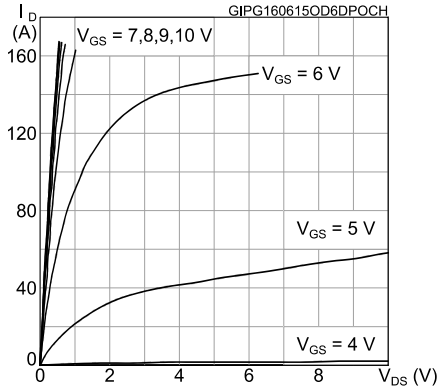


Figure 5: Transfer characteristics

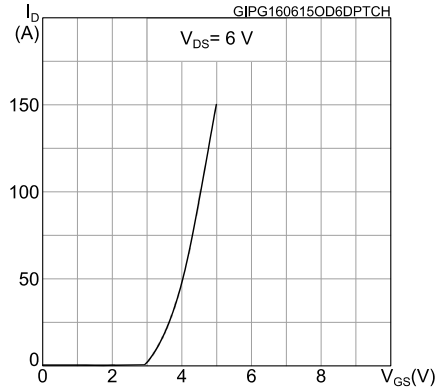


Figure 6: Gate charge vs gate-source voltage

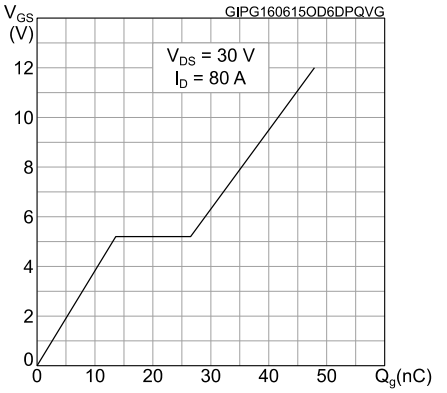


Figure 7: Static drain-source on-resistance