



STU9NC80Z STU9NC80ZI

N-CHANNEL 800V - 0.82Ω - 8.6A Max220/I-Max220
Zener-Protected PowerMESH™III MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STU9NC80Z	800 V	<0.9Ω	8.6 A
STU9NC80ZI	800 V	<0.9Ω	8.6 A

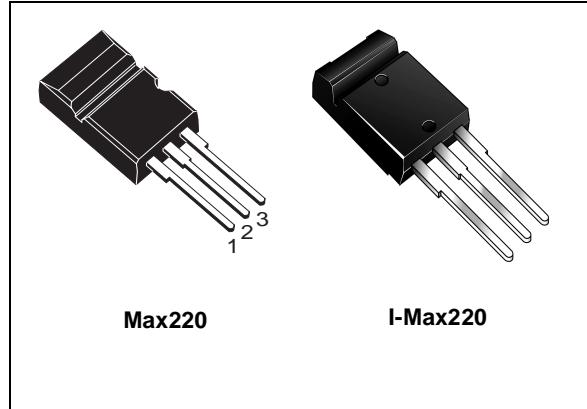
- TYPICAL R_{DS(on)} = 0.82Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- GATE-TO-SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

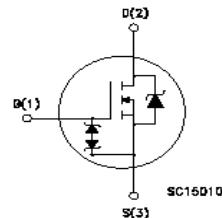
The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS,
COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STU9NC80Z	STU9NC80ZI	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	800	800	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	800	800	V
V _{GS}	Gate- source Voltage	±25	±25	V
I _D	Drain Current (continuos) at T _C = 25°C	8.6	8.6(*)	A
I _D	Drain Current (continuos) at T _C = 100°C	5.4	5.4(*)	A
I _{DM} (1)	Drain Current (pulsed)	34.4	34.4(*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	160	55	W
	Derating Factor	1.28	0.44	W/°C
I _{GS}	Gate-source Current	±50	±50	mA
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=15kΩ)	4	4	kV
dv/dt(•)	Peak Diode Recovery voltage slope	3	3	V/ns
V _{ISO}	Insulation Winthstand Voltage (DC)	--	2000	V
T _{stg}	Storage Temperature	−65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤ 8.6A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

(*)Limited only by maximum temperature allowed

STU9NC80Z/STU9NC80ZI

THERMAL DATA

		Max220	I-Max220	
Rthj-case	Thermal Resistance Junction-case Max	0.78	2.27	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30		°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	8.6	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	400	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	800			V
ΔV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 1 mA, V _{GS} = 0		1		V/°C
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±10	μA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{D(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 4.7A		0.82	0.9	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{D(on)max} , V _{GS} = 10V	8.6			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward Transconductance	V _{DS} > I _{D(on)} × R _{D(on)max} , I _D = 4.7A		13		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		3500		pF
C _{oss}	Output Capacitance			230		pF
C _{rss}	Reverse Transfer Capacitance			25		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON (RESISTIVE LOAD)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 400V, I_D = 4.5A$		35		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		16		ns
Q_g	Total Gate Charge	$V_{DD} = 640V, I_D = 9A, V_{GS} = 10V$		72.2	101	nC
Q_{gs}	Gate-Source Charge			19.5		nC
Q_{gd}	Gate-Drain Charge			24.3		nC

SWITCHING OFF (INDUCTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 640V, I_D = 9A, R_G = 4.7\Omega, V_{GS} = 10V$		32		ns
t_f	Fall Time			42		ns
t_c	Cross-over Time	(see test circuit, Figure 5)		67		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				8.6	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				34.4	A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 8.6A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 9A, dI/dt = 100A/\mu s, V_{DD} = 100V, T_j = 150^\circ C$		730		ns
Q_{rr}	Reverse Recovery Charge			7.2		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		19.5		A

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1mA$ (Open Drain)	25			V
αT	Voltage Thermal Coefficient	$T = 25^\circ C$ Note(3)		1.3		$10^{-4}/^\circ C$
R_z	Dynamic Resistance	$I_{GS} = 50mA, V_{GS} = 0$		90		Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

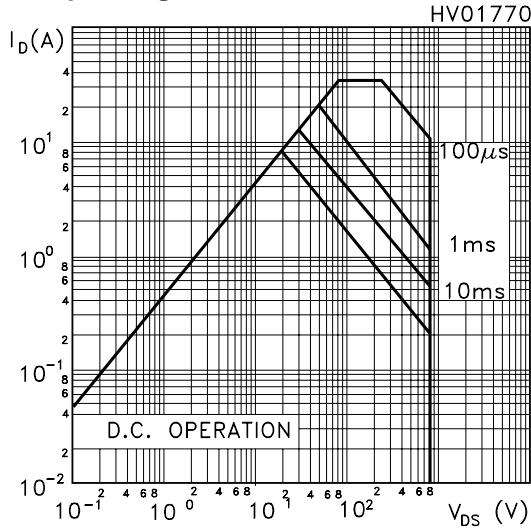
3. $\Delta V_{BV} = \alpha T (25^\circ - T) BV_{GSO}(25^\circ)$

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

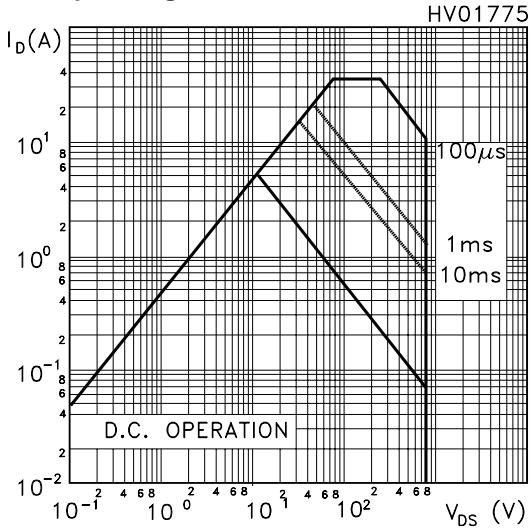
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STU9NC80Z/STU9NC80ZI

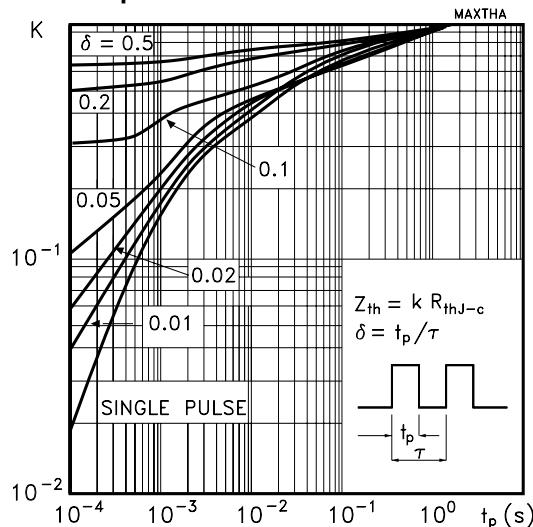
Safe Operating Area For Max220



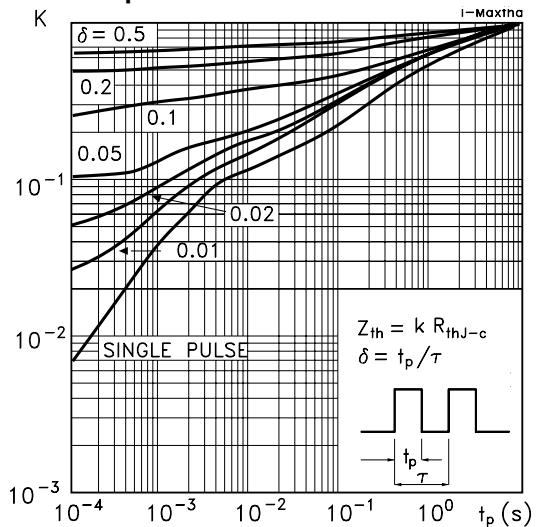
Safe Operating Area For I-Max220



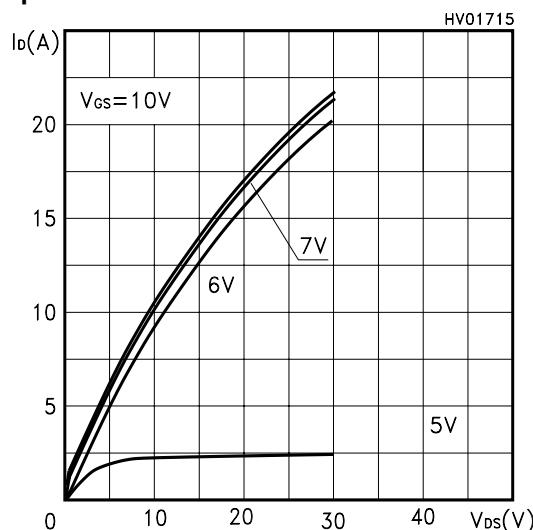
Thermal Impedance For Max220



Thermal Impedance For I-Max220



Output Characteristics



Transfer Characteristics

