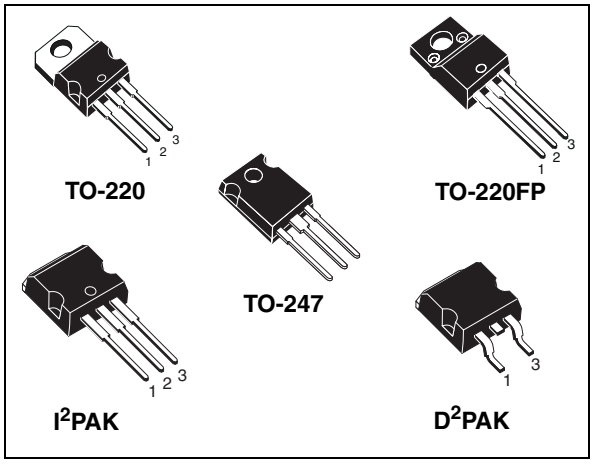
STP14NK50Z - STP14NK50ZFP
STB14NK50Z-STB14NK50Z-1-STW14NK50Z

N-channel 500V - 0.34Ω - 14A TO-220/FP/D^{2}PAK/I^{2}PAK/TO-247
Zener-protected SuperMESH^{TM} Power MOSFET

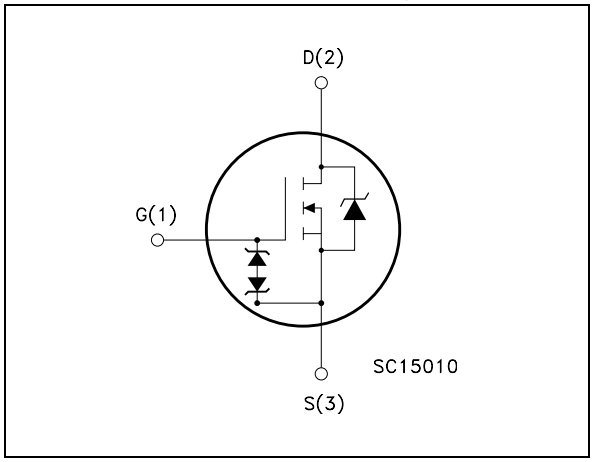
General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP14NK50Z	500V	<0.38Ω	14A	150W
STP14NK50ZFP	500V	<0.38Ω	14A	35W
STB14NK50Z	500V	<0.38Ω	14A	150W
STB14NK50Z-1	500V	<0.38Ω	14A	150W
STW14NK50Z	500V	<0.38Ω	14A	150W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility



Internal schematic diagram



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP14NK50Z	P14NK50Z	TO-220	Tube
STP14NK50ZFP	P14NK50ZFP	TO-220FP	Tube
STB14NK50ZT4	B14NK50Z	D^{2}PAK	Tape & reel
STB14NK50Z-1	B14NK50Z	I^{2}PAK	Tube
STW14NK50Z	W14NK50Z	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220 I^2PAK/D^2PAK	TO-220FP	TO-247	
V_{DS}	Drain-source voltage (V_{GS} = 0)	500			V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	500			V
V_{GS}	Gate-source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25°C	14	14(1)	14	A
I_D	Drain current (continuous) at T_C=100°C	7.6	7.6(1)	7.6	A
I_{DM}(2)	Drain current (pulsed)	48	48(1)	48	A
P_{TOT}	Total dissipation at T_C = 25°C	150	35	150	W
	Derating factor	1.20	0.28	1.20	W/°C
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5kΩ)	4000			KV
dv/dt(3)	Peak diode recovery voltage slope	4.5			V/ns
V_{ISO}	Insulation withstand voltage (DC)	--	2500		V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 3A$, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		TO-220 I^2PAK	D^2PAK	TO-220FP	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	0.83		3.6	0.83	°C/W
Rthj-pcb	Thermal resistance junction-pcb Max (1)		60			°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5			50	°C/W
T_l	Maximum lead temperature for soldering purpose	300				°C

1. When mounted on minimum footprint

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	12	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	400	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=±1mA (Open Drain)	30			V

1.1 Protection features og gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, T_C =125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 100µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 6A		0.34	0.38	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =8V, I_D = 6A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		2000 238 55		pF pF pF
$C_{oss\ eq}$(2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 400V		150		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=400V, I_D = 12A V_{GS} =10V		69 12 31	92	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=250 V, I_D=6A, R_G=4.7Ω, V_{GS}=10V (see Figure 19)		24 16		ns ns

Table 7. Switching times

$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=250V, I_D=6A, R_G=4.7Ω, V_{GS}=10V (see Figure 19)		54 12		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD}=400 V, I_D=12A, R_G=4.7Ω, V_{GS}=10V (see Figure 21)		9.5 9 20		ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				12	A
I_{SDM}(1)	Source-drain current (pulsed)				48	A
V_{SD}(2)	Forward on voltage	I_{SD}=12A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=12A, di/dt = 100A/µs, V_{DD}=35V, Tj=150°C (see Figure 21)		470 3.1 13.2		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

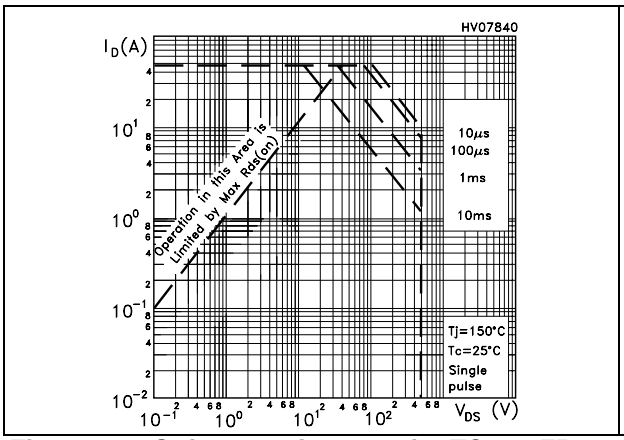


Figure 2. Thermal impedance

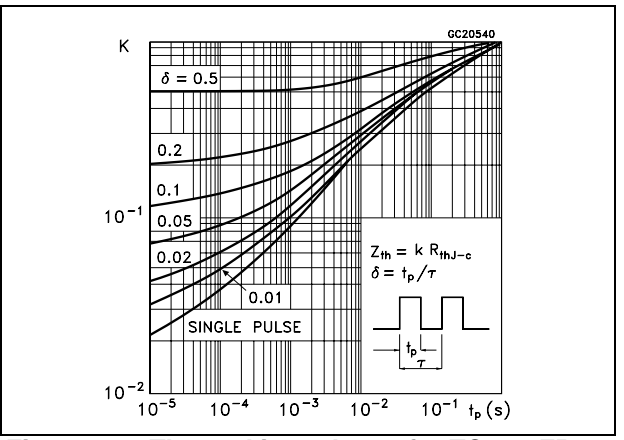


Figure 3. Safe operating area for TO-220FP

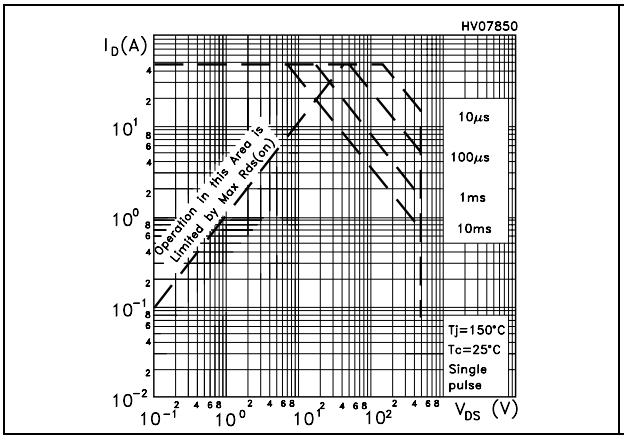


Figure 4. Thermal impedance for TO-220FP

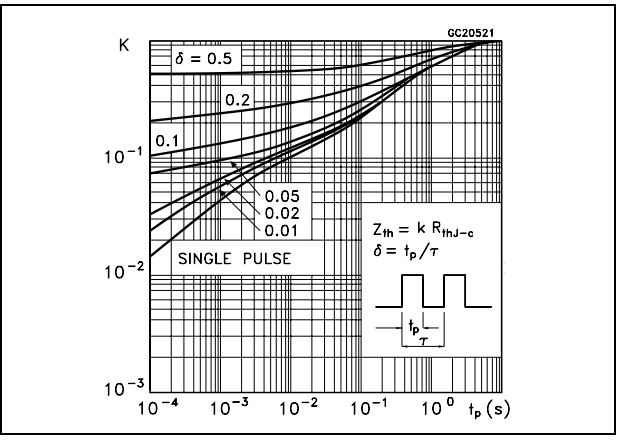


Figure 5. Safe operating area for TO-247

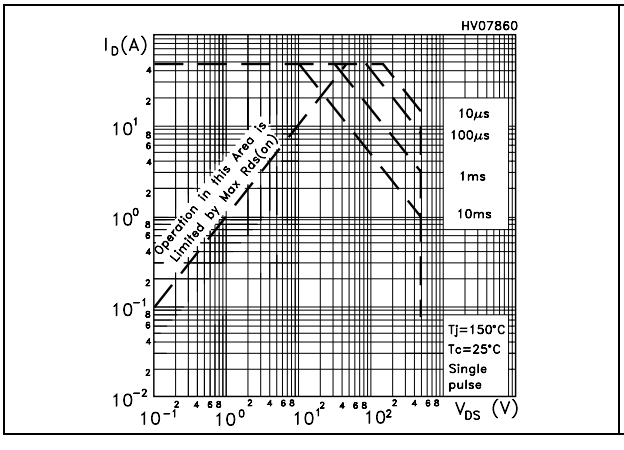
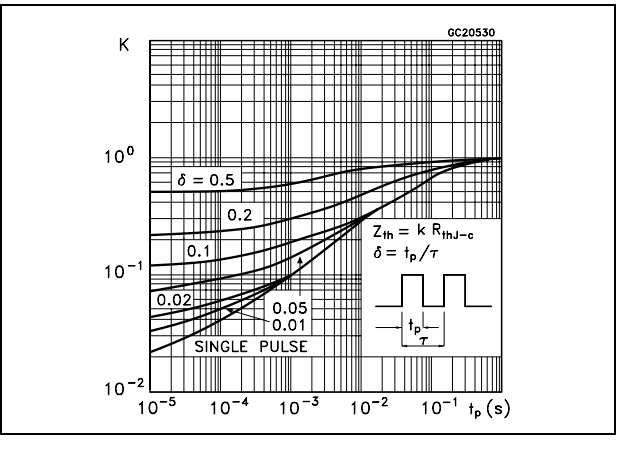



Figure 6. Thermal impedance for TO-247