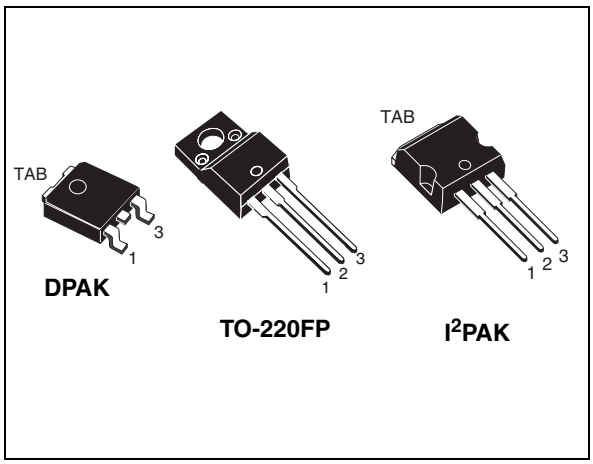
STD5N52U
STF5N52U, STI5N52U

N-channel 525 V, 1.28 Ω, 4.4 A, DPAK, TO-220FP, I²PAK UltraFASTmesh™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STD5N52U	525 V	< 1.5 Ω	4.4 A	70 W
STF5N52U				25 W
STI5N52U				70 W

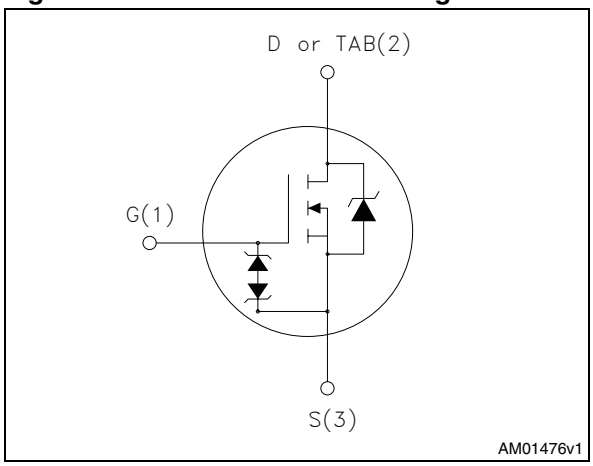
- 100% avalanche tested
- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low $R_{DS(on)}$
- Extremely low t_{rr}



Applications

- Switching applications
  - High voltage inverters specific fo LCD TV
  - Lighting full bridge topology
  - Motor control

Figure 1. Internal schematic diagram



Description

These devices are N-channel Power MOSFETs developed using UltraFASTmesh™ technology, which combines the advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD5N52U	5N52U	DPAK	Tape and reel
STF5N52U	5N52U	TO-220FP	Tube
STI5N52U	5N52U	I²PAK	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	I^2PAK	
V_{GS}	Gate- source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25 °C	4.4			A
I_D	Drain current (continuous) at T_C = 100 °C	2.8			A
I_{DM} (1)	Drain current (pulsed)	17.6			A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.4			A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170			mJ
dv/dt(2)	Peak diode recovery voltage slope	20			V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM C=100 pF; R=1.5 kΩ)	2800			V
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)		2500		V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 4.4 A, di/dt ≤ 400 A/µs, peak V_{DS} ≤$V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	I^2PAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.78	5	1.78	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		62.5	100	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb	50			°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 525 V V_{DS} = 525 V, T_C=125 °C			10 500	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.2 A		1.28	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	529 71 13.4	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 420 V, V_{GS} = 0	-	11	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	6	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 416 V, I_D = 4.4 A, V_{GS} = 10 V	-	16.9 4.2 8.4	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 260 V, I_D = 2.2 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	11.4 13.6 23.1 15	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		4.4 17.6	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.4 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V	-	55 95 3.5		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C	-	120 266 4.5		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and I^2PAK

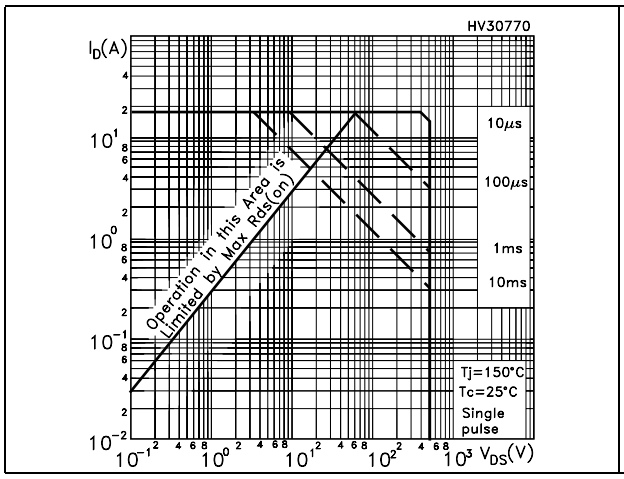


Figure 3. Thermal impedance for DPAK and I^2PAK

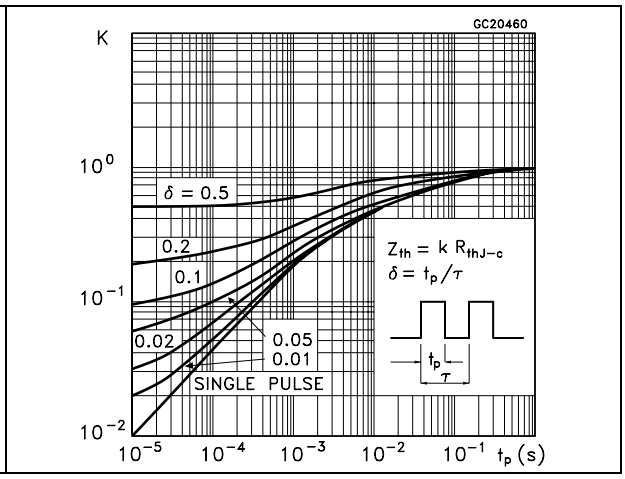


Figure 4. Safe operating area for TO-220FP

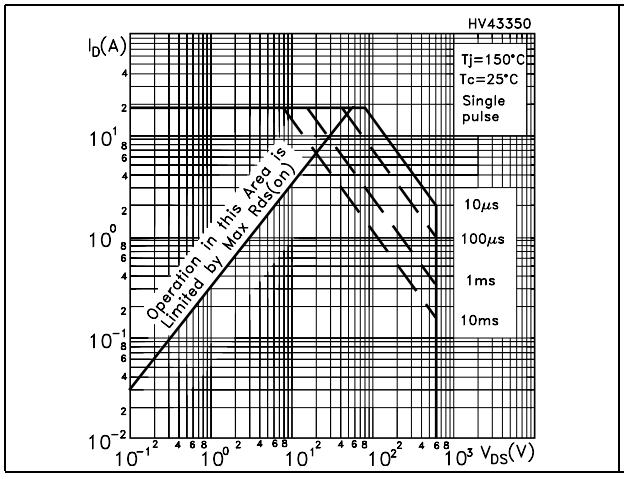


Figure 5. Thermal impedance for TO-220FP

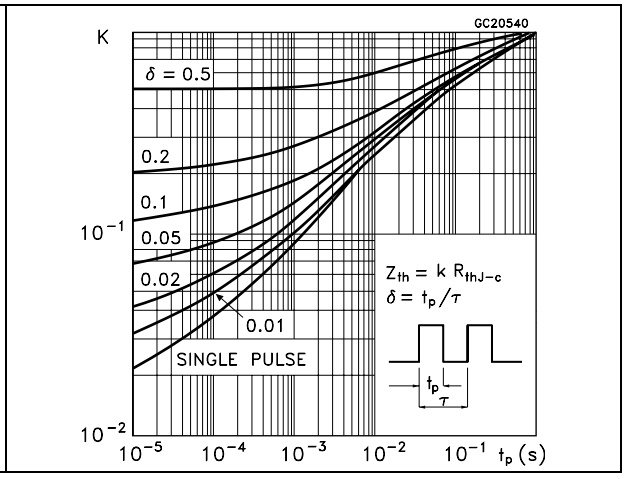


Figure 6. Output characteristics

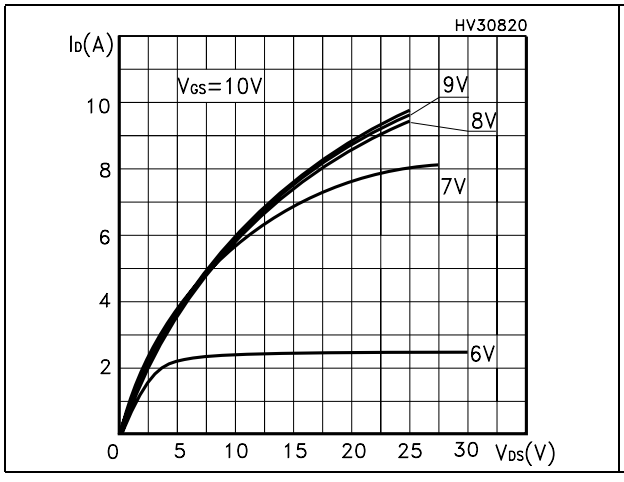
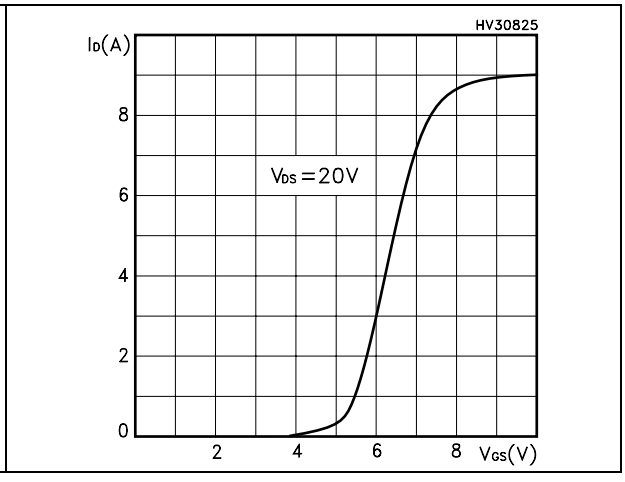



Figure 7. Transfer characteristics