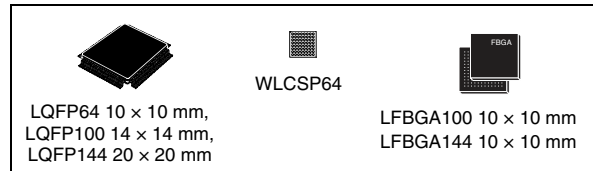


# STM32F103xC STM32F103xD STM32F103xE

High-density performance line ARM-based 32-bit MCU with 256 to 512KB Flash, USB, CAN, 11 timers, 3 ADCs, 13 communication interfaces

## Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 256 to 512 Kbytes of Flash memory
  - up to 64 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V<sub>BAT</sub> supply for RTC and backup registers
- 3 × 12-bit, 1 μs A/D converters (up to 21 channels)
  - Conversion range: 0 to 3.6 V
  - Triple-sample and hold capability
  - Temperature sensor
- 2 × 12-bit D/A converters
- DMA: 12-channel DMA controller
  - Supported peripherals: timers, ADCs, DAC, SDIO, I<sup>2</sup>Ss, SPIs, I<sup>2</sup>Cs and USARTs
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M3 Embedded Trace Macrocell™



- Up to 112 fast I/O ports
  - 51/80/112 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- Up to 11 timers
  - Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 × 16-bit motor control PWM timers with dead-time generation and emergency stop
  - 2 × watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 × 16-bit basic timers to drive the DAC
- Up to 13 communication interfaces
  - Up to 2 × I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 3 SPIs (18 Mbit/s), 2 with I<sup>2</sup>S interface multiplexed
  - CAN interface (2.0B Active)
  - USB 2.0 full speed interface
  - SDIO interface
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

**Table 1. Device summary**

Reference	Part number
STM32F103xC	STM32F103RC STM32F103VC STM32F103ZC
STM32F103xD	STM32F103RD STM32F103VD STM32F103ZD
STM32F103xE	STM32F103RE STM32F103ZE STM32F103VE

## 5.2 Absolute maximum ratings

**Table 7. Voltage characteristics**

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup>	-0.3	4.0	V
$V_{IN}$ <sup>(2)</sup>	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins		50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)			

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.

**Table 8. Current characteristics**

Symbol	Ratings	Max.	Unit
$I_{VDD}$	Total current into $V_{DD}/V_{DDA}$ power lines (source) <sup>(1)</sup>	150	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	150	
$I_{IO}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ <sup>(2)</sup>	Injected current on five volt tolerant pins <sup>(3)</sup>	-5/+0	
	Injected current on any other pin <sup>(4)</sup>	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) <sup>(5)</sup>	± 25	

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.

**Table 9. Thermal characteristics**

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	–65 to +150	°C
$T_J$	Maximum junction temperature	150	°C

## 5.3 Operating conditions

### 5.3.1 General operating conditions

**Table 10. General operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency		0	72	MHz
$f_{PCLK1}$	Internal APB1 clock frequency		0	36	
$f_{PCLK2}$	Internal APB2 clock frequency		0	72	
$V_{DD}$	Standard operating voltage		2	3.6	V
$V_{DDA}^{(1)}$	Analog operating voltage (ADC not used)	Must be the same potential as $V_{DD}^{(2)}$	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
$V_{BAT}$	Backup operating voltage		1.8	3.6	V
$P_D$	Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 <sup>(3)</sup>	LQFP144		666	mW
		LQFP100		434	
		LQFP64		444	
		LFBGA100		500	
		LFBGA144		500	
		WLCSP64		400	
$T_A$	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation <sup>(4)</sup>	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation <sup>(4)</sup>	–40	125	
$T_J$	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

### 5.3.2 Operating conditions at power-up / power-down

**Table 11. Operating conditions at power-up / power-down**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate		0	$\infty$	$\mu\text{s/V}$
	$V_{DD}$ fall time rate		20	$\infty$	

### 5.3.3 Embedded reset and power control block characteristics

**Table 12. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(1)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}^{(2)}$	PDR hysteresis			40		mV
$T_{RSTTEMPO}^{(2)}$	Reset temporization		1	2.5	4.5	mS

1. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

2. Guaranteed by design, not tested in production.

**Table 20. Peripheral current consumption<sup>(1)</sup> (continued)**

Peripheral		Typical consumption at 25 °C	Unit
APB2	GPIOA	0.55	mA
	GPIOB	0.72	
	GPIOC	0.72	
	GIOD	0.55	
	GPIOE	1	
	GPIOF	0.72	
	GPIOG	1	
	ADC1 <sup>(2)</sup>	1.9	
	ADC2	1.7	
	TIM1	1.8	
	SPI1	0.4	
	TIM8	1.7	
	USART1	0.9	
	ADC3	1.7	

1.  $f_{HCLK} = 72 \text{ MHz}$ ,  $f_{APB1} = f_{HCLK}/2$ ,  $f_{APB2} = f_{HCLK}$ , default prescaler value for each peripheral.

2. Specific conditions for ADC:  $f_{HCLK} = 56 \text{ MHz}$ ,  $f_{APB1} = f_{HCLK}/2$ ,  $f_{APB2} = f_{HCLK}$ ,  $f_{ADCLK} = f_{APB2}/4$ , ADON bit in the ADC\_CR2 register is set to 1.

### 5.3.6 External clock source characteristics

#### High-speed external user clock generated from an external source

**Table 21. High-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	User external clock source frequency <sup>(1)</sup>		1	8	25	MHz
$V_{HSEH}$	OSC_IN input pin high level voltage		$0.7V_{DD}$		$V_{DD}$	V
$V_{HSEL}$	OSC_IN input pin low level voltage		$V_{SS}$		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time <sup>(1)</sup>		5			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time <sup>(1)</sup>				20	
$C_{in(HSE)}$	OSC_IN input capacitance <sup>(1)</sup>			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
$I_L$	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu A$

1. Guaranteed by design, not tested in production.

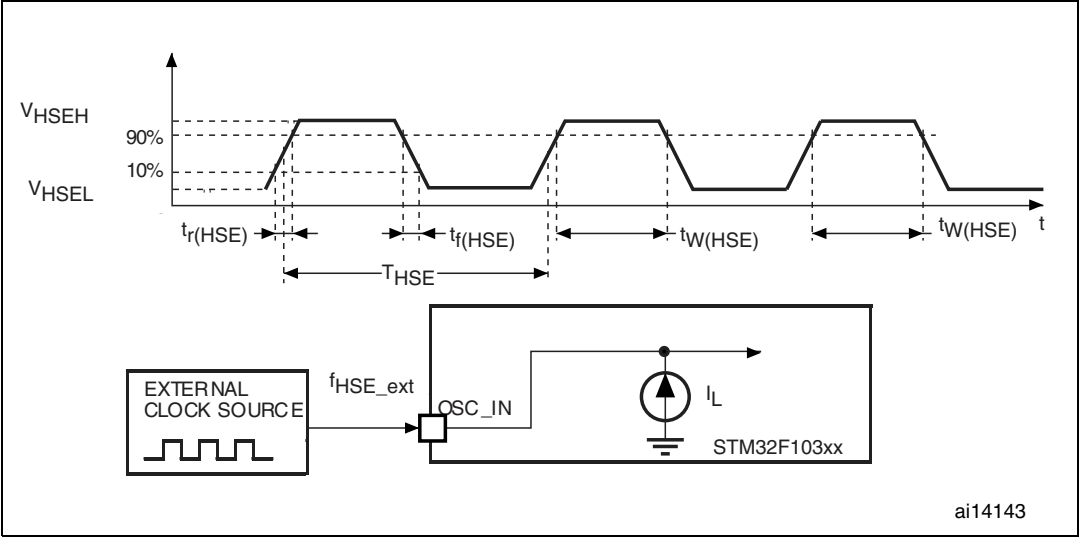
Low-speed external user clock generated from an external source

Table 22. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User External clock source frequency <sup>(1)</sup>			32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		$0.7V_{DD}$		$V_{DD}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		$V_{SS}$		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time <sup>(1)</sup>		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time <sup>(1)</sup>				50	
$C_{in(LSE)}$	OSC32_IN input capacitance <sup>(1)</sup>			5		pF
DuCy(LSE)	Duty cycle		30		70	%
$I_L$	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_D$			$\pm 1$	$\mu A$

1. Guaranteed by design, not tested in production.

Figure 20. High-speed external clock source AC timing diagram



### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in . In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

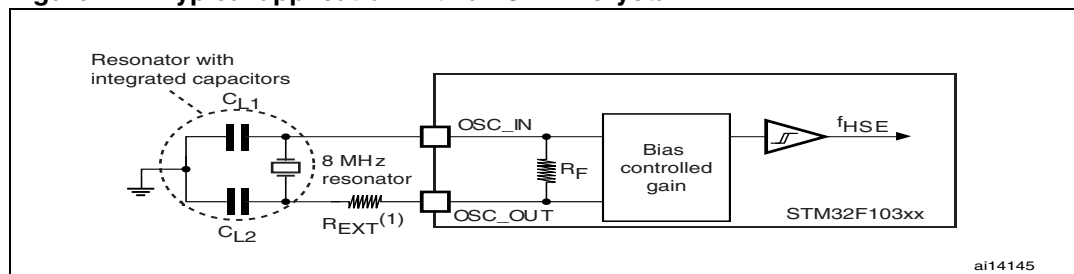
**Table 23. HSE 4-16 MHz oscillator characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	8	16	MHz
$R_F$	Feedback resistor			200		k $\Omega$
C	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(3)</sup>	$R_S = 30 \Omega$		30		pF
$i_2$	HSE driving current	$V_{DD} = 3.3 \text{ V}$ , $V_{IN} = V_{SS}$ with 30 pF load			1	mA
$g_m$	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE)}$ <sup>(4)</sup>	Startup time	$V_{DD}$ is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see ).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

**Figure 22. Typical application with an 8 MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics.

## 5.3.14 I/O port characteristics

## General input/output characteristics

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Standard IO input low level voltage		-0.3		$0.28 \cdot (V_{DD} - 2 \text{ V}) + 0.8 \text{ V}$	V
	IO FT <sup>(1)</sup> input low level voltage		-0.3		$0.32 \cdot (V_{DD} - 2 \text{ V}) + 0.75 \text{ V}$	V
$V_{IH}$	Standard IO input high level voltage		$0.41 \cdot (V_{DD} - 2 \text{ V}) + 1.3 \text{ V}$		$V_{DD} + 0.3$	V
	IO FT <sup>(1)</sup> input high level voltage	$V_{DD} > 2 \text{ V}$	$0.42 \cdot (V_{DD} - 2 \text{ V}) + 1 \text{ V}$		5.5	V
		$V_{DD} \leq 2 \text{ V}$			5.2	
$V_{hys}$	Standard IO Schmitt trigger voltage hysteresis <sup>(2)</sup>		200			mV
	IO FT Schmitt trigger voltage hysteresis <sup>(2)</sup>		$5\% V_{DD}$ <sup>(3)</sup>			mV
$I_{lkg}$	Input leakage current <sup>(4)</sup>	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			$\pm 1$	$\mu\text{A}$
		$V_{IN} = 5 \text{ V}$ , I/O FT			3	
$R_{PU}$	Weak pull-up equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$R_{PD}$	Weak pull-down equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{DD}$	30	40	50	$k\Omega$
$C_{IO}$	I/O pin capacitance			5		pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than  $V_{DD} + 0.3$  the internal pull-up/pull-down resistors must be disabled.

2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

3. With a minimum of 100 mV.

4. Leakage could be higher than max. if negative current is injected on adjacent pins.

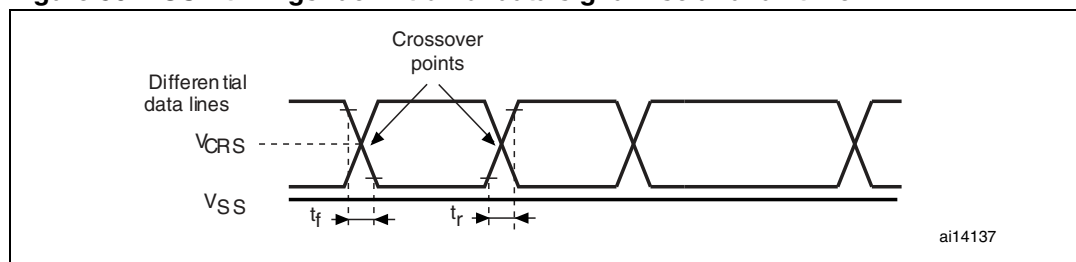
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).



**Table 57. USB DC electrical characteristics**

Symbol	Parameter	Conditions	Min. <sup>(1)</sup>	Max. <sup>(1)</sup>	Unit
Input levels					
V <sub>DD</sub>	USB operating voltage <sup>(2)</sup>		3.0 <sup>(3)</sup>	3.6	V
V <sub>DI</sub> <sup>(4)</sup>	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
V <sub>CM</sub> <sup>(4)</sup>	Differential common mode range	Includes V <sub>DI</sub> range	0.8	2.5	
V <sub>SE</sub> <sup>(4)</sup>	Single ended receiver threshold		1.3	2.0	
Output levels					
V <sub>OL</sub>	Static output level low	R <sub>L</sub> of 1.5 kΩ to 3.6 V <sup>(5)</sup>		0.3	V
V <sub>OH</sub>	Static output level high	R <sub>L</sub> of 15 kΩ to V <sub>SS</sub> <sup>(5)</sup>	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 k $\Omega$  resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V  $V_{DD}$  voltage range.
4. Guaranteed by characterization, not tested in production.
5.  $R_L$  is the load connected on the USB drivers

**Figure 56. USB timings: definition of data signal rise and fall time****Table 58. USB: full-speed electrical characteristics**

<b>Driver characteristics<sup>(1)</sup></b>					
Symbol	Parameter	Conditions	Min	Max	Unit
$t_r$	Rise time <sup>(2)</sup>	$C_L = 50$ pF	4	20	ns
$t_f$	Fall Time <sup>(2)</sup>	$C_L = 50$ pF	4	20	ns
$t_{rfm}$	Rise/ fall time matching	$t_r/t_f$	90	110	%
$V_{CRS}$	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

### 5.3.19 12-bit ADC characteristics

*Note: It is recommended to perform a calibration after each power-up.*

**Table 59. ADC characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	Power supply		2.4		3.6	V
$V_{REF+}$	Positive reference voltage		2.4		$V_{DDA}$	V
$I_{VREF}$	Current on the $V_{REF}$ input pin			160 <sup>(1)</sup>	220	$\mu A$
$f_{ADC}$	ADC clock frequency		0.6		14	MHz
$f_S^{(2)}$	Sampling rate		0.05		1	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 14 \text{ MHz}$			823	kHz
					17	$1/f_{ADC}$
$V_{AIN}$	Conversion voltage range <sup>(3)</sup>		0 ( $V_{SSA}$ or $V_{REF-}$ tied to ground)		$V_{REF+}$	V
$R_{AIN}^{(2)}$	External input impedance				50	k $\Omega$
$R_{ADC}^{(2)}$	Sampling switch resistance				1	k $\Omega$
$C_{ADC}^{(2)}$	Internal sample and hold capacitor				8	pF
$t_{CAL}^{(2)}$	Calibration time	$f_{ADC} = 14 \text{ MHz}$	5.9			$\mu s$
			83			$1/f_{ADC}$
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 14 \text{ MHz}$			0.214	$\mu s$
					3 <sup>(4)</sup>	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 14 \text{ MHz}$			0.143	$\mu s$
					2 <sup>(4)</sup>	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 14 \text{ MHz}$	0.107		17.1	$\mu s$
			1.5		239.5	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time		0	0	1	$\mu s$
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 14 \text{ MHz}$	1		18	$\mu s$
			14 to 252 ( $t_S$ for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.

2. Guaranteed by design, not tested in production.

### 5.3.20 DAC electrical specifications

**Table 63. DAC characteristics**

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$V_{DDA}$	Analog supply voltage	2.4		3.6	V	
$V_{REF+}$	Reference supply voltage	2.4		3.6	V	$V_{REF+}$ must always be below $V_{DDA}$
$V_{SSA}$	Ground	0		0	V	
$R_{LOAD}^{(1)}$	Resistive load with buffer ON	5			k $\Omega$	
$R_O^{(1)}$	Impedance output with buffer OFF			15	k $\Omega$	When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 M $\Omega$
$C_{LOAD}^{(1)}$	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min <sup>(1)</sup>	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x155) and (0xEAB) at $V_{REF+} = 2.4$ V
DAC_OUT max <sup>(1)</sup>	Higher DAC_OUT voltage with buffer ON			$V_{DDA} - 0.2$	V	
DAC_OUT min <sup>(1)</sup>	Lower DAC_OUT voltage with buffer OFF		0.5		mV	It gives the maximum output excursion of the DAC.
DAC_OUT max <sup>(1)</sup>	Higher DAC_OUT voltage with buffer OFF			$V_{REF+} - 1\text{LSB}$	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)			220	$\mu$ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
$I_{DDA}$	DAC DC current consumption in quiescent mode (Standby mode)			380	$\mu$ A	With no load, middle code (0x800) on the inputs
				480	$\mu$ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
DNL <sup>(2)</sup>	Differential non linearity Difference between two consecutive code-1LSB)			$\pm 0.5$	LSB	Given for the DAC in 10-bit configuration
				$\pm 2$	LSB	Given for the DAC in 12-bit configuration
INL <sup>(2)</sup>	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)			$\pm 1$	LSB	Given for the DAC in 10-bit configuration
				$\pm 4$	LSB	Given for the DAC in 12-bit configuration

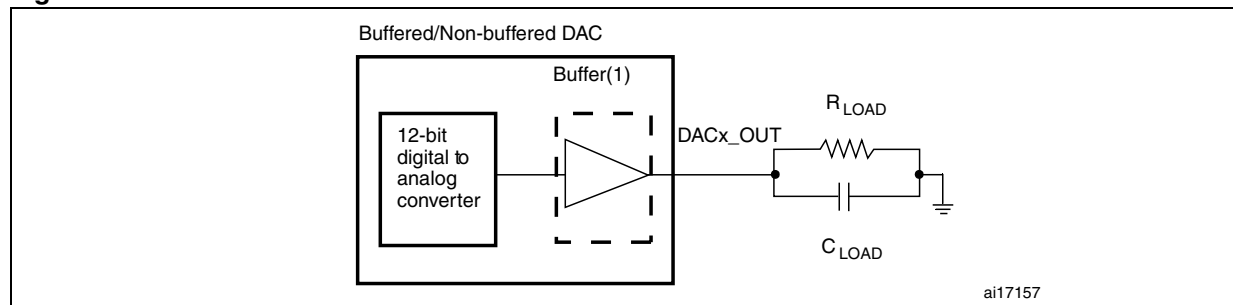
Table 63. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset <sup>(2)</sup>	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$ )			±10	mV	Given for the DAC in 12-bit configuration
				±3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6\text{ V}$
				±12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6\text{ V}$
Gain error <sup>(2)</sup>	Gain error			±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}^{(2)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB)		3	4	μs	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$
Update rate <sup>(2)</sup>	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$
$t_{WAKEUP}^{(2)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)		6.5	10	μs	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ <sup>(1)</sup>	Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)		-67	-40	dB	No $R_{LOAD}$ , $C_{LOAD} = 50\text{ pF}$

1. Guaranteed by design, not tested in production.

2. Guaranteed by characterization, not tested in production.

Figure 61. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.