

CD4063B Types

CMOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

■ CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A_3, B_3 , through A_0, B_0), three outputs ($A < B, A = B, A > B$) and three cascading inputs ($A < B, A = B, A > B$) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: ($A < B$) = low, ($A = B$) = high, ($A > B$) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs ($A < B, A = B$, and $A > B$) on the least significant comparator are connected to a low, a high, and a low level, respectively.

The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix). This device is pin-compatible with the standard 7485 TTL type.

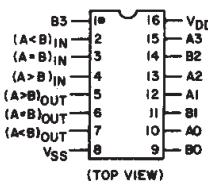
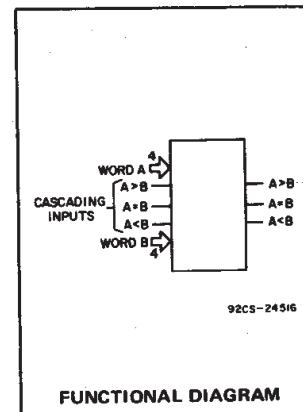
Features:

- Expansion to 8, 12, 16...4N bits by cascading units
- Medium-speed operation:
compares two 4-bit words
in 250 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V
over full package temperature range;
100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
range) = 1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Servo motor controls ■ Process controllers



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

±10mA

POWER DISSIPATION PER PACKAGE (PD):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

100mW

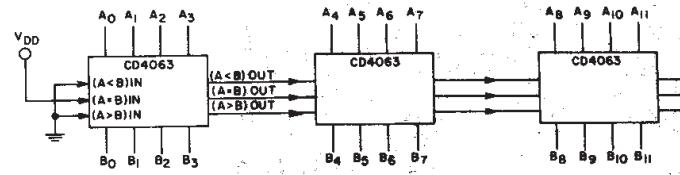
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ -55°C to $+125^\circ\text{C}$

OPERATING-TEMPERATURE RANGE (T_A) -65°C to $+150^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79mm) from case for 10s, max +265°C



$$t_p \text{ TOTAL} = t_p \text{ (COMPARE)} + 2 \times t_p \text{ (CASCADE)}, \text{ AT } V_{DD} = 10V \\ (3 \text{ STAGES})$$

= 250 + (2 × 200) = 650 ns (TYP.)

Fig. 1 — Typical speed characteristics of a 12-bit comparator.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-}\text{Temperature Range}$)	3	18	V

CD4063B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			Min.	Typ.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0,04	5	—	—	μA
	—	0,10	10	10	10	300	300	—	0,04	10	—	—	
	—	0,15	15	20	20	600	600	—	0,04	20	—	—	
	—	0,20	20	100	100	3000	3000	—	0,08	100	—	—	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	—	—	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	—	—	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	—	—	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	—	—	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	—	—	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	—	—	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	—	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0,05				—	0	0,05	—	—	V
	—	0,10	10	0,05				—	0	0,05	—	—	
	—	0,15	15	0,05				—	0	0,05	—	—	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4,95				4,95	5	—	—	—	V
	—	0,10	10	9,95				9,95	10	—	—	—	
	—	0,15	15	14,95				14,95	15	—	—	—	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	—	5	1,5				—	—	1,5	—	—	V
	1,9	—	10	3				—	—	3	—	—	
	1,5,13,5	—	15	4				—	—	4	—	—	
Input High Voltage, V _{IH} Min.	0,5, 4,5	—	5	3,5				3,5	—	—	—	—	V
	1,9	—	10	7				7	—	—	—	—	
	1,5,13,5	—	15	11				11	—	—	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA	—	—

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

TRUTH TABLE

INPUTS				OUTPUTS					
COMPARING				CASCAADING					
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	A < B	A = B	A > B	A < B	A = B	A > B
A ₃ > B ₃	X	X	X	X	X	X	0	0	1
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	0	0	1	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	0	1	0	0	1	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	1	0	0	1	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	1	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	1	0	0
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	1	0	0
A ₃ < B ₃	X	X	X	X	X	X	1	0	0

X = Don't Care

Logic 1 ≡ High Level

Logic 0 ≡ Low Level

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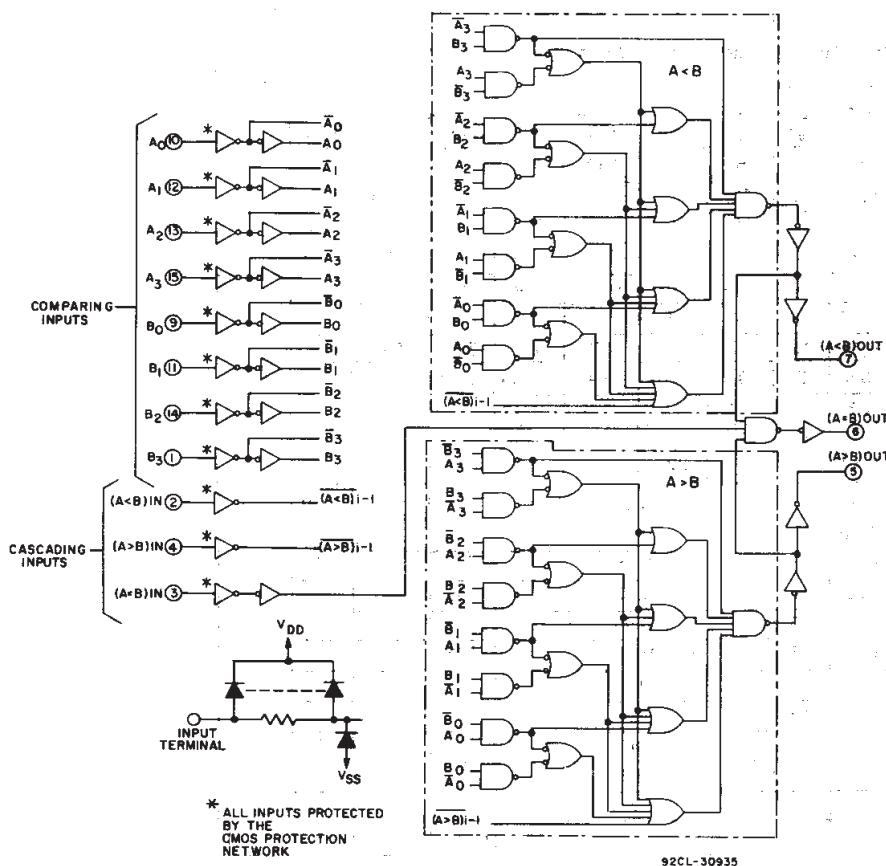


Fig. 2 – Logic diagram for CD4063B.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_p, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{k}\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
	V _{DD} Volts		Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t _{PHL} , t _{PLH}	5	625	1250		ns
	10	250	500		
	15	175	350		
Cascading Inputs to Outputs, t _{PHL} , t _{PLH}	5	500	1000		
	10	200	400		
	15	140	280		
Transition Time, t _{THL} , t _{T LH}	5	100	200		ns
	10	50	100		
	15	40	80		
Input Capacitance, C _{IN}	Any Input	5	7.5	pF	

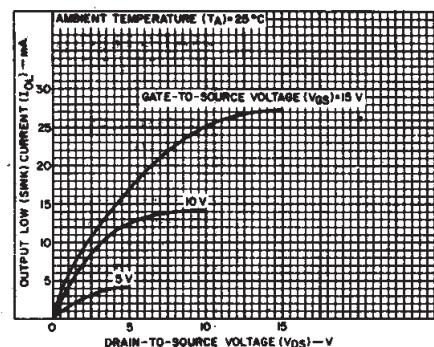


Fig. 3 – Typical output low (sink) current characteristics.

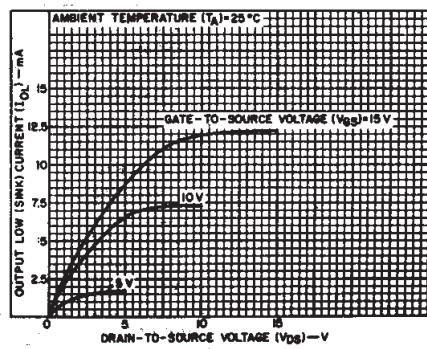


Fig. 4 – Minimum output low (sink) current characteristics.

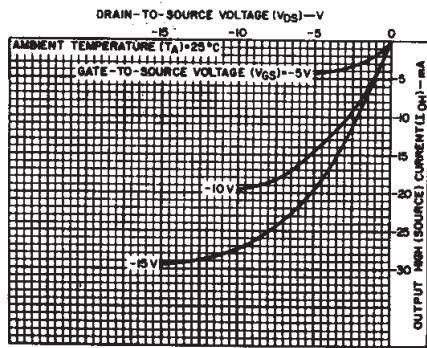


Fig. 5 – Typical output high (source) current characteristics.

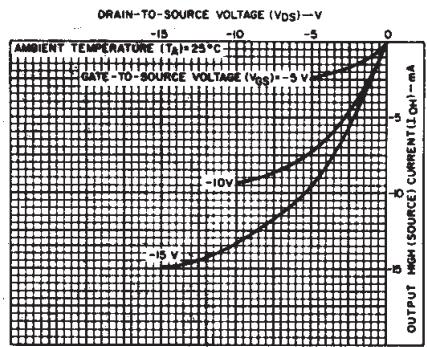
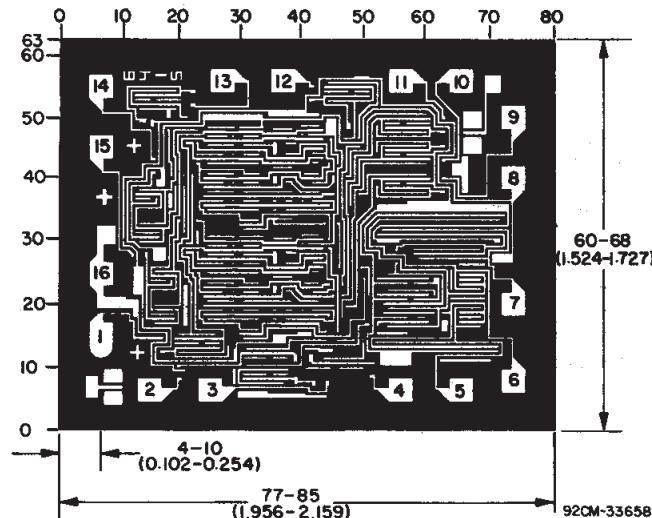
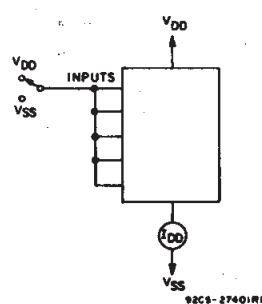
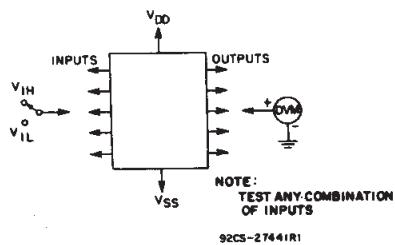
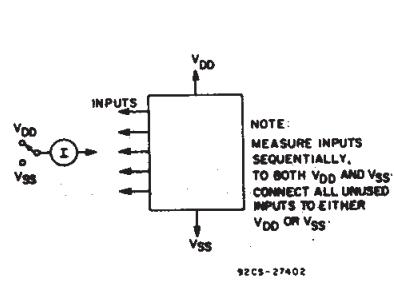
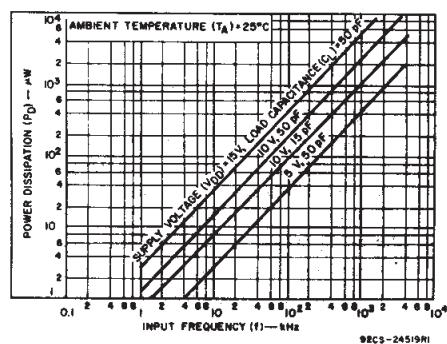
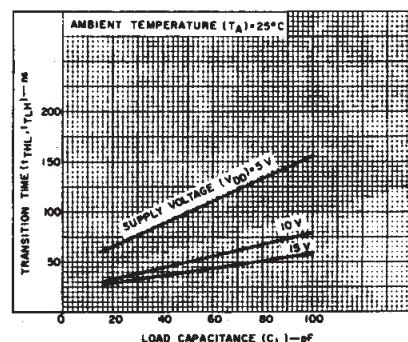
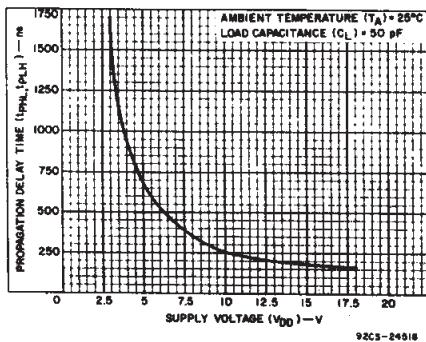
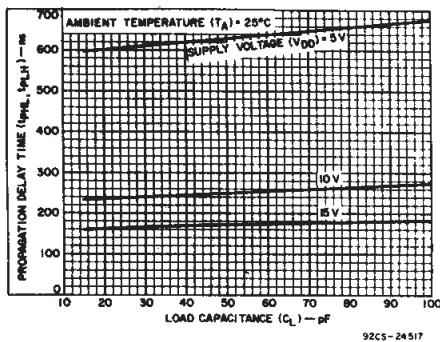


Fig. 6 – Minimum output high (source) current characteristics.

CD4063B Types



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).