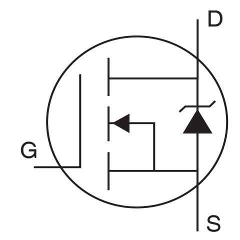
IRF1404PbF

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Automotive Qualified (Q101)
- Lead-Free

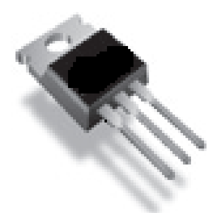
Power MOSFET



V_{DSS} = 40V

$R_{DS(on)}$ = 0.004Ω

I_D = 202A⑥



TO-220AB

Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications including automotive.

The TO-220 package is universally preferred for all automotive-commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

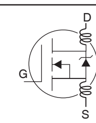
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	202⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	143⑥	
I_{DM}	Pulsed Drain Current ①	808	
P_D @T_C = 25°C	Power Dissipation	333	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	620	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

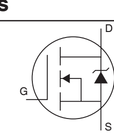
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.039	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0035	0.004	Ω	V_{GS} = 10V, I_D = 121A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	76	—	—	S	V_{DS} = 25V, I_D = 121A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	131	196	nC	I_D = 121A
Q_{gs}	Gate-to-Source Charge	—	36	—		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	37	56		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 20V
t_r	Rise Time	—	190	—		I_D = 121A
$t_{d(off)}$	Turn-Off Delay Time	—	46	—		R_G = 2.5Ω
t_f	Fall Time	—	33	—		R_D = 0.2Ω ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5669	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1659	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	223	—		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	6205	—		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	1467	—		V_{GS} = 0V, V_{DS} = 32V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	2249	—		V_{GS} = 0V, V_{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	202⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	808		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J = 25°C, I_S = 121A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	78	117	ns	T_J = 25°C, I_F = 121A
Q_{rr}	Reverse RecoveryCharge	—	163	245	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 85μH R_G = 25Ω, I_{AS} = 121A. (See Figure 12)

③ $I_{SD} \leq$ 121A, di/dt ≤ 130A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

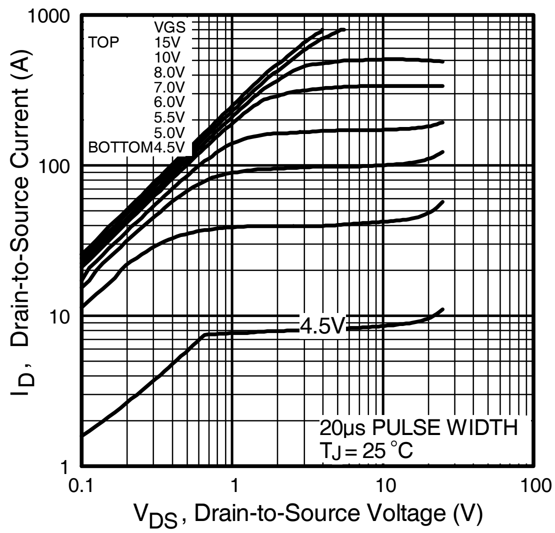


Fig 1. Typical Output Characteristics

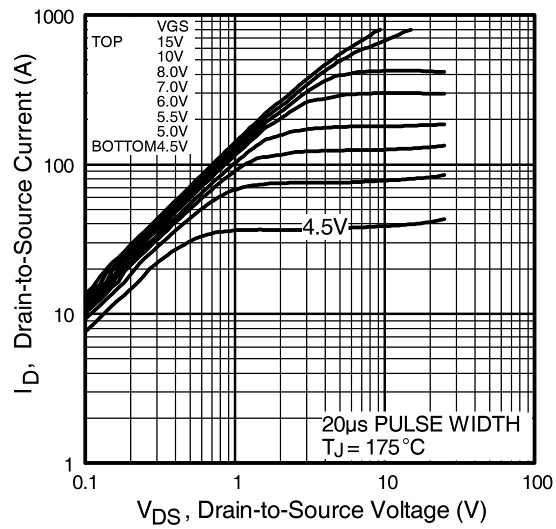


Fig 2. Typical Output Characteristics

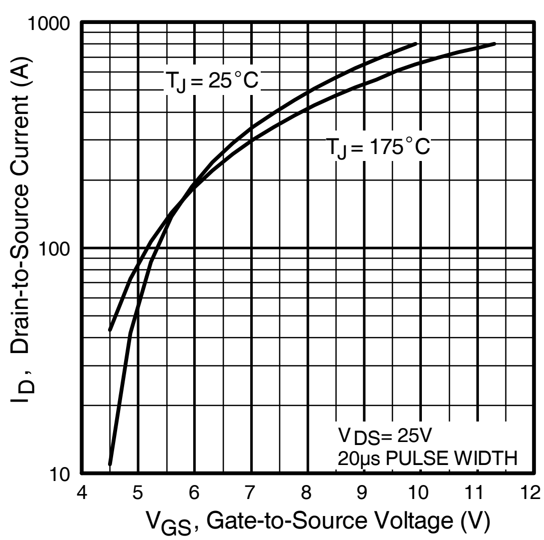


Fig 3. Typical Transfer Characteristics

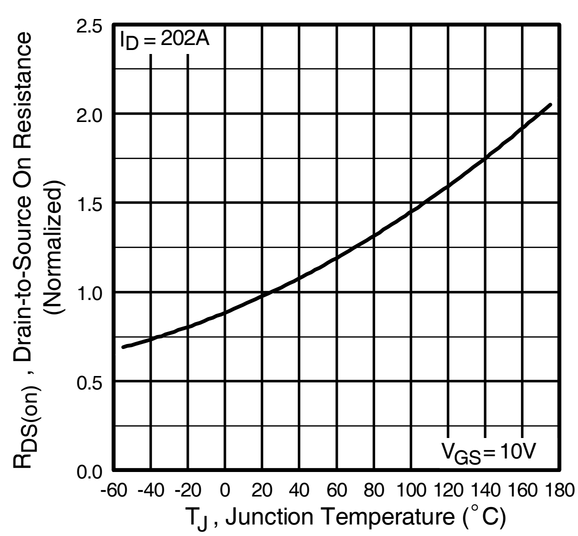


Fig 4. Normalized On-Resistance Vs. Temperature

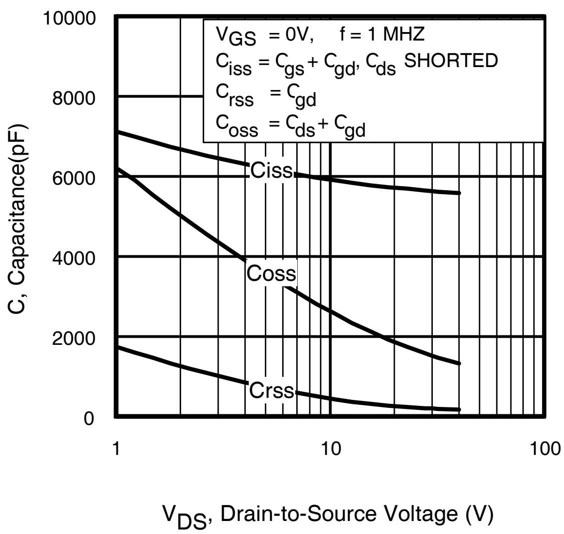


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

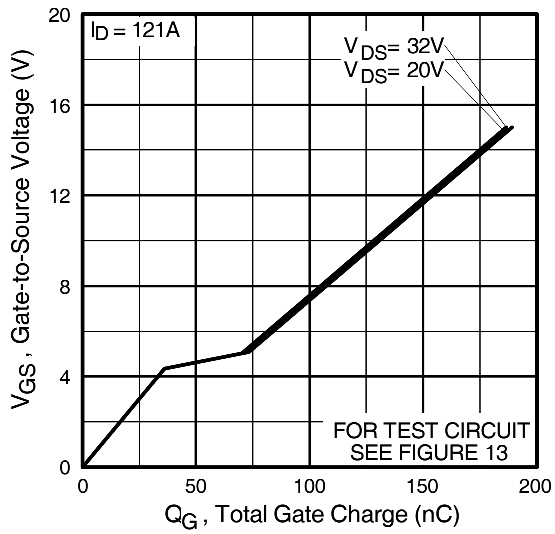


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

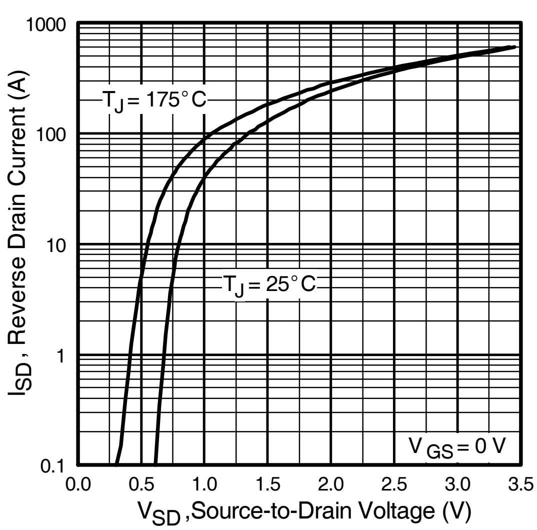


Fig 7. Typical Source-Drain Diode Forward Voltage

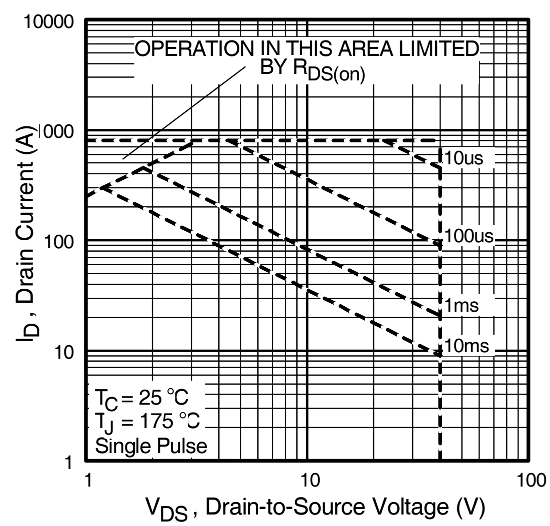


Fig 8. Maximum Safe Operating Area

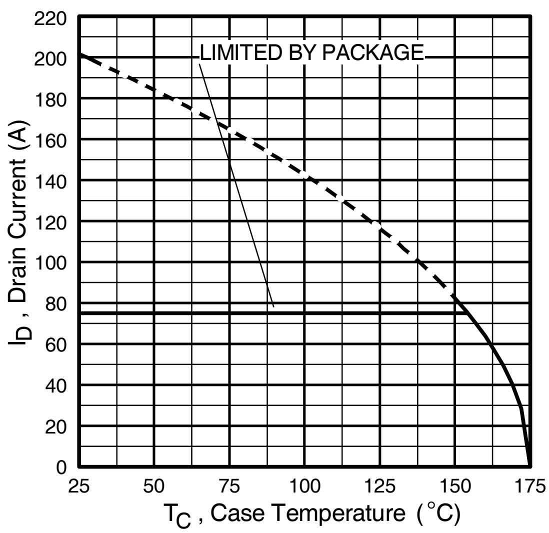


Fig 9. Maximum Drain Current Vs. Case Temperature

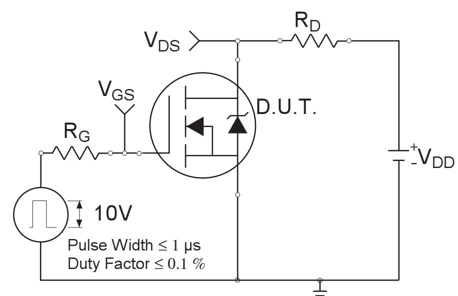


Fig 10a. Switching Time Test Circuit

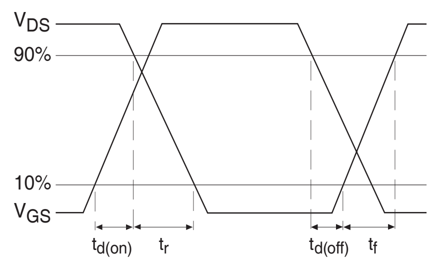


Fig 10b. Switching Time Waveforms

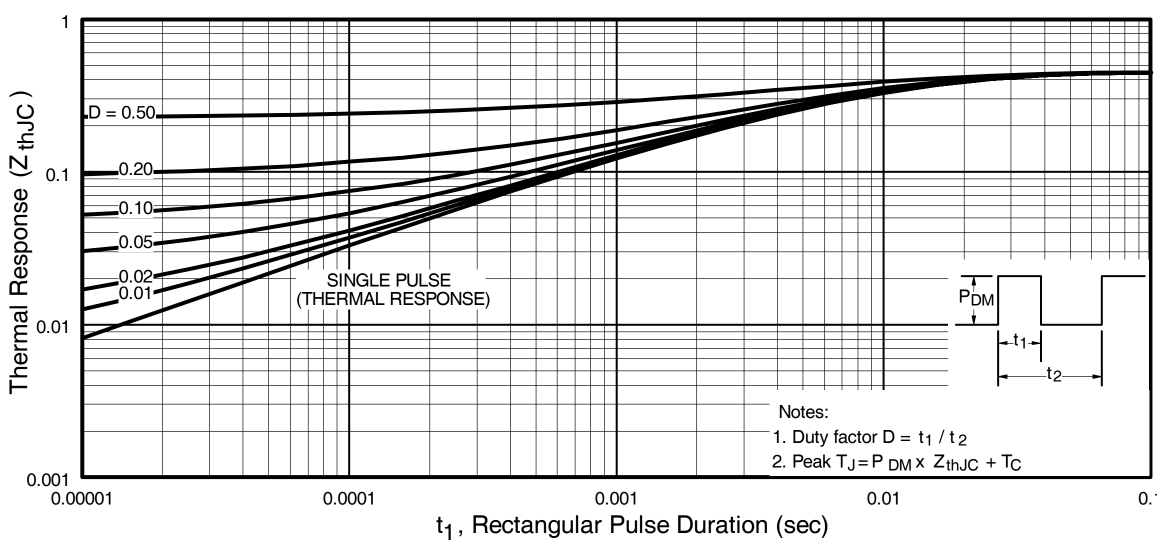


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

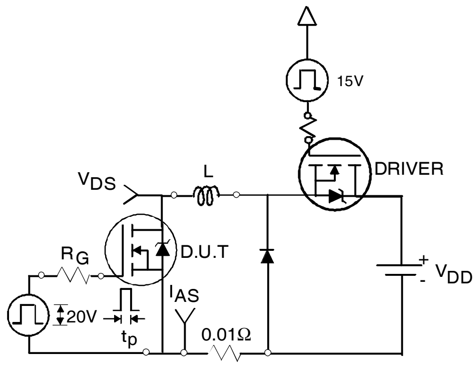


Fig 12a. Unclamped Inductive Test Circuit

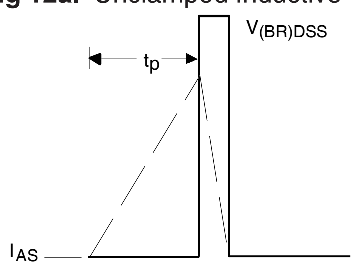


Fig 12b. Unclamped Inductive Waveforms

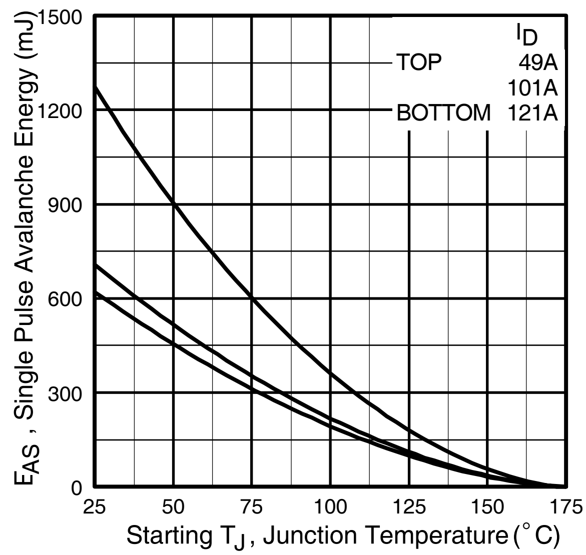


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

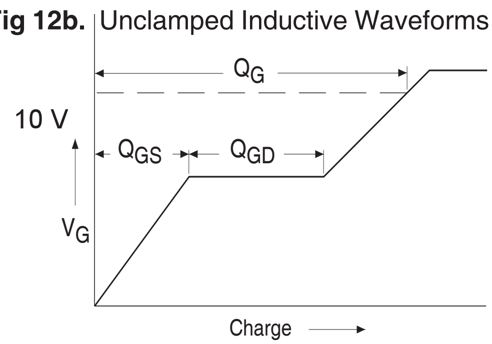


Fig 13a. Basic Gate Charge Waveform

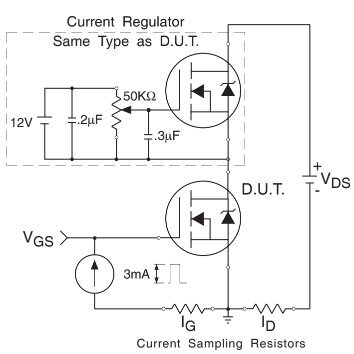


Fig 13b. Gate Charge Test Circuit

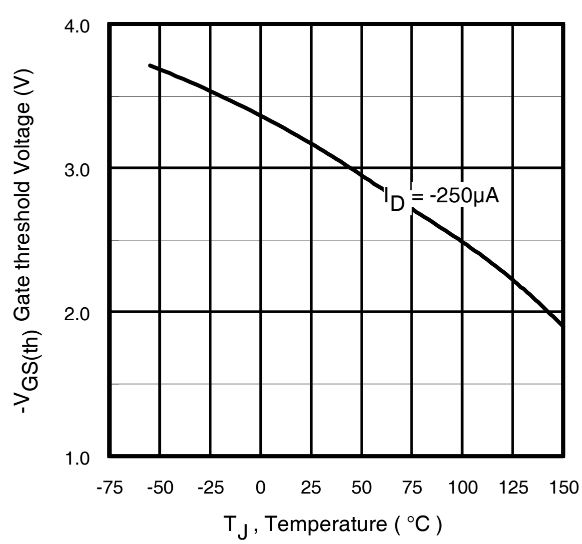


Fig 14. Threshold Voltage Vs. Temperature

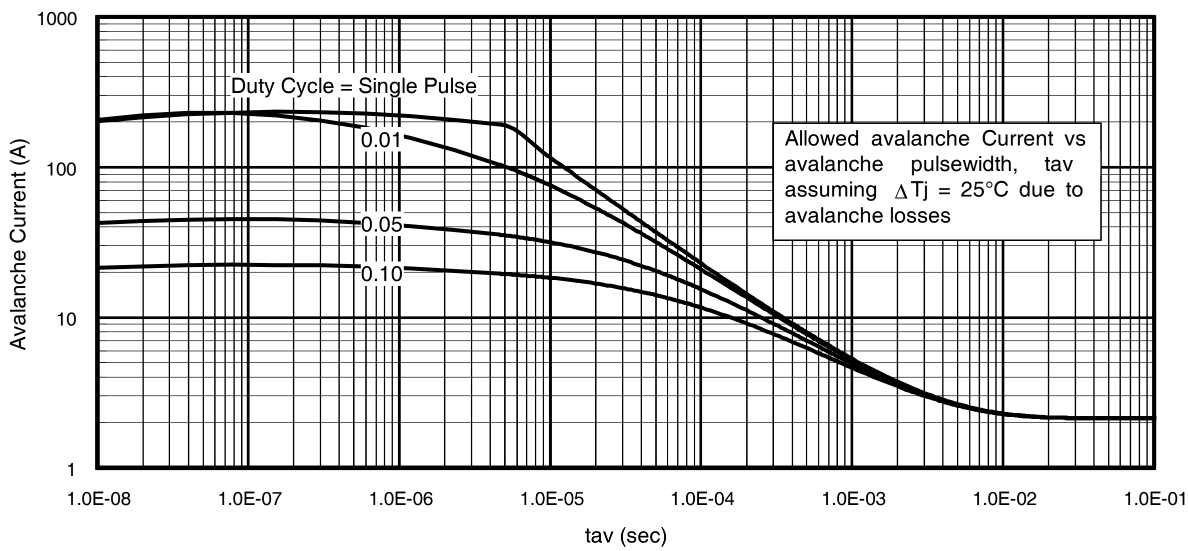


Fig 15. Typical Avalanche Current Vs.Pulsewidth

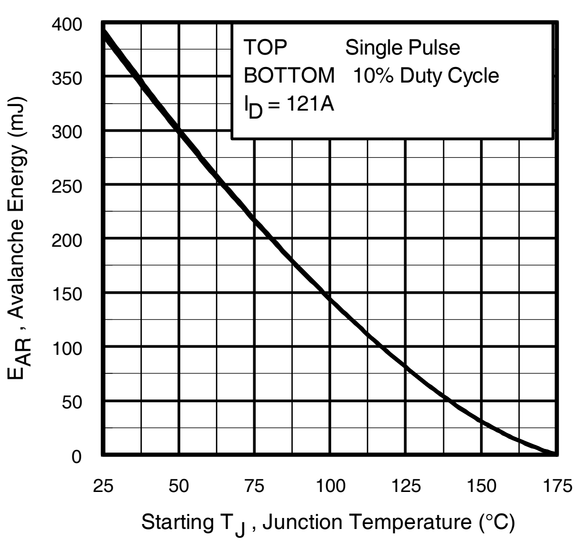
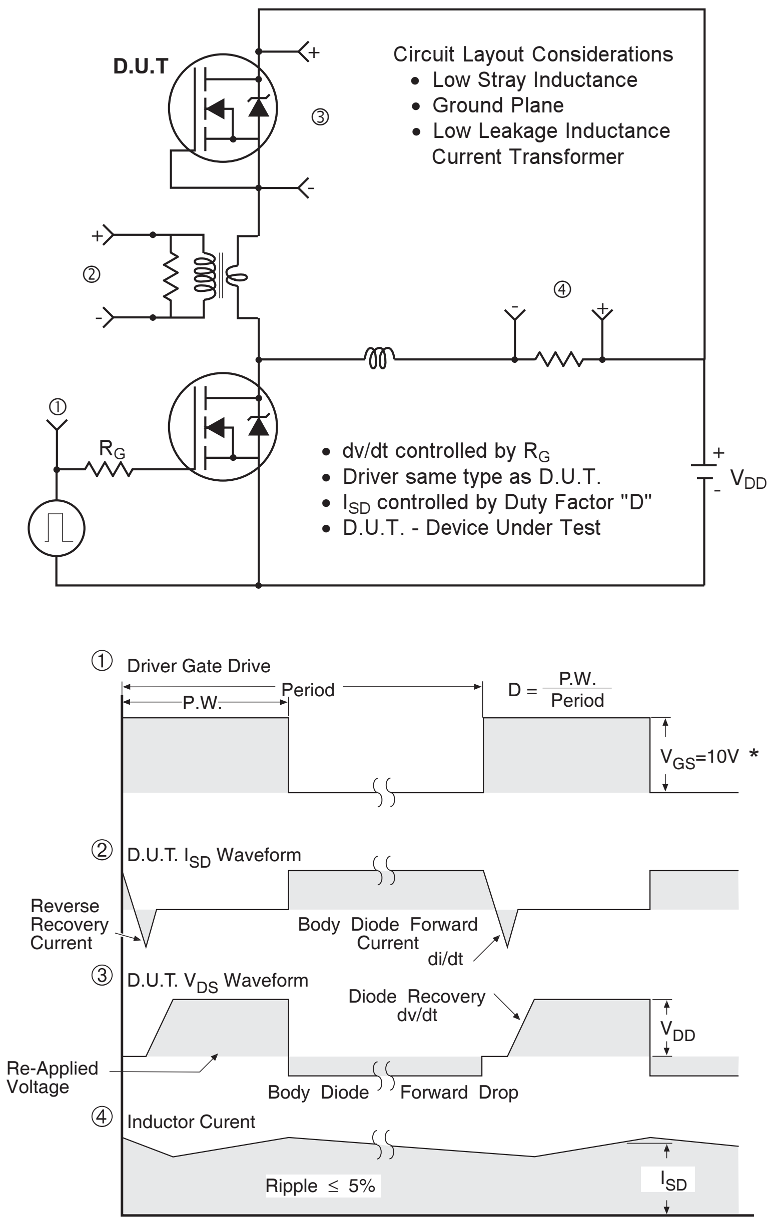


Fig 16. Maximum Avalanche Energy Vs. Temperature

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$\mathbf{P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}}$$
$$\mathbf{I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]}$$
$$\mathbf{E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}}$$

Peak Diode Recovery dv/dt Test Circuit

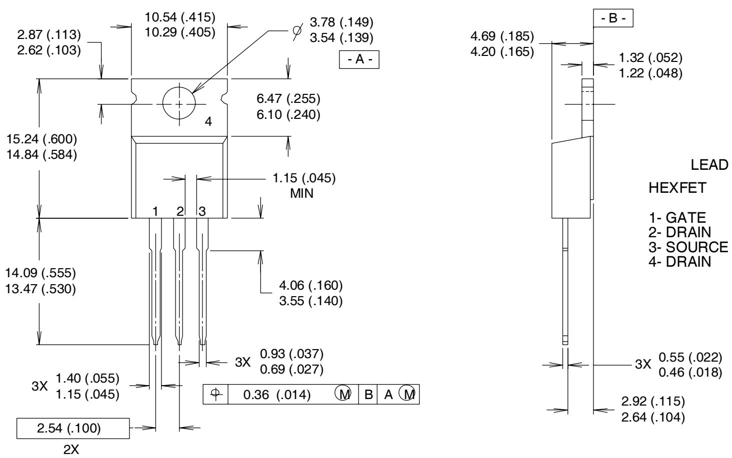


* V_{GS} = 5V for Logic Level Devices

Fig 17. For N-channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"