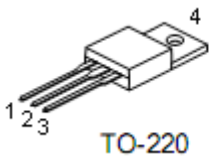
1. Description

These N-Channel enhancement mode power field effect transistors are produced using KIA's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

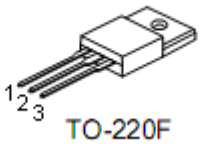
2. Features

- 65A, 60V, $R_{DS(on)}$= 0.016Ω @V_{GS}= 10 V
- Low gate charge (typical 48nC)
- Low Crss (typical 32.5pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175° maximum junction temperature rating

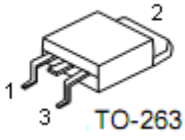
3. Pin configuration



TO-220



TO-220F



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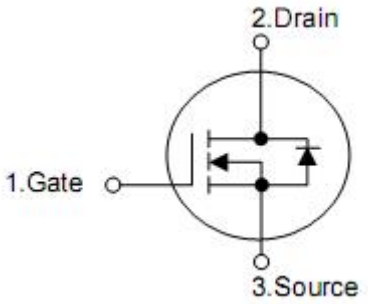


Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise specified)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	60	V
Drain current	Tc=25 ºC	I_D	65	A
	Tc=100 ºC		40	A
Drain current pulsed (note 1)		I_{DM}	260	A
Gate-source voltage		V_{GSS}	±20	V
Single pulsed avalanche energy (note 2)		E_{AS}	650	mJ
Avalanche current (note 1)		I_{AR}	65	A
Repetitive avalanche energy (note 1)		E_{AR}	15.0	mJ
Peak diode recovery dv/dt (note 3)		dv/dt	7.0	V/ns
Power dissipation	Tc=25 ºC	P_D	150	W
	derate above 25 ºC		1.00	W/ºC
Operating and Storage temperature range		T_J , T_{STG}	-55 ~ +175	ºC
Maximum lead temperature for soldering purposes,1/8” from case for 5 seconds		T_L	300	ºC

5. Thermal characteristics

Parameter	Symbol	Min	Max	Unit
Thermal resistance,Junction-to-case	$R_{\theta JC}$		1.00	ºC /W
Thermal resistance,case-to-sink	$R_{\theta CS}$	0.5		ºC /W
Thermal resistance,Junction-to-ambient	$R_{\theta JA}$		62.5	ºC /W

6. Electrical characteristics

(T_J=25°C,unless otherwise notes)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics							
Drain-source breakdown voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	60			V
Breakdown voltage temperature coefficient		$\Delta BV_{DSS}/\Delta T_J$	I_D=250μA, referenced to 25 ºC		0.07		V/ºC
Zero gate voltage drain current		I_{DSS}	V_{DS}=60V ,V_{GS}=0V			1	μA
			V_{DS}=48V ,T_C=150ºC			10	μA
Gate-body leakage current	Forward	I_{GSSF}	V_{GS}=20V,V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-20V,V_{DS}=0V			-100	nA
On characteristics							
Gate threshold voltage		$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static drain-source on-resistance		$R_{DS(on)}$	V_{GS}=10V,I_D=39A		0.015	0.016	Ω
Forward transconductance		g_{FS}	V_{DS}=25V, I_D=32.5A (note4)			100	S
Dynamic characteristics							
Input capacitance		C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz		2000		pF
Output capacitance		C_{oss}			450		pF
Reverse transfer capacitance		C_{rss}			32.5		pF
Switching characteristics							
Turn-on delay time		$t_{d(on)}$	V_{DD}=30V,I_D=39A,R_G=4.7Ω R_D=0.77Ω,V_{GS}=10V (note4,5)		12		ns
Turn-on rise time		t_r			33		ns
Turn-off delay time		$t_{d(off)}$			41		ns
Turn-off fall time		t_f			12		ns
Total gate charge		Q_g	V_{DS}=30V, I_D=39A,V_{GS}=10V, (note4,5)		40		nC
Gate-source charge		Q_{gs}			8		nC
Gate-drain charge		Q_{gd}			12		nC
Drain-source diode characteristics and maximum rating							
Maximum continuous drain-source diode forward current		I_S				65	A
Maximum pulsed drain-source diode forward current		I_{SM}				260	A
Drain-source diode forward voltage		V_{SD}	V_{GS}=0V,I_S=65A			1.5	V
Reverse recovery time		t_{rr}	V_{GS}=0V,I_S=65A dI_F/dt=100A/μs (note4)		60		ns
Reverse recovery charge		Q_{rr}			100		μC

Note:1.repetitive rating:pulse width limited by maximum junction temperature

2.L=180μH,I_{AS}=65A,V_{DD}=25V,R_G=25Ω,staring T_J=25ºC

3.I_{SD}≤65A,di/dt≤100A/μs,V_{DD}≤BV_{DSS},staring T_J=25 ºC

4.Pulse test:pulse width≤300μs,duty cycle≤2%

5.Essentially independent of operating temperature

7 . Test circuits and waveforms

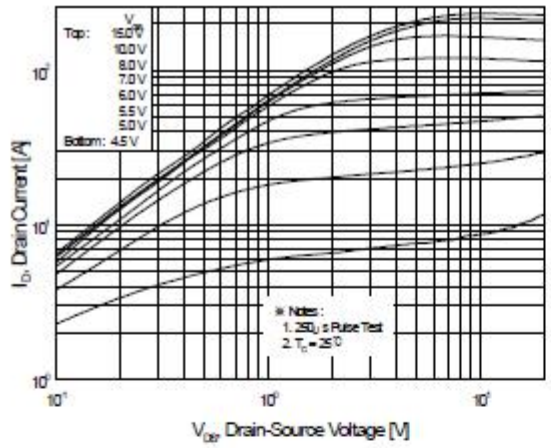


Figure 1. On-Region Characteristics

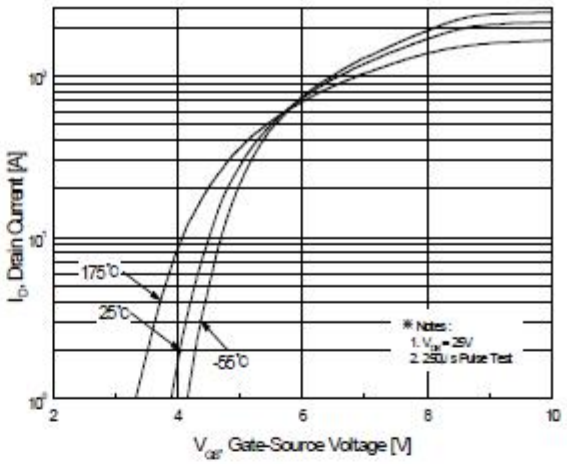


Figure 2. Transfer Characteristics

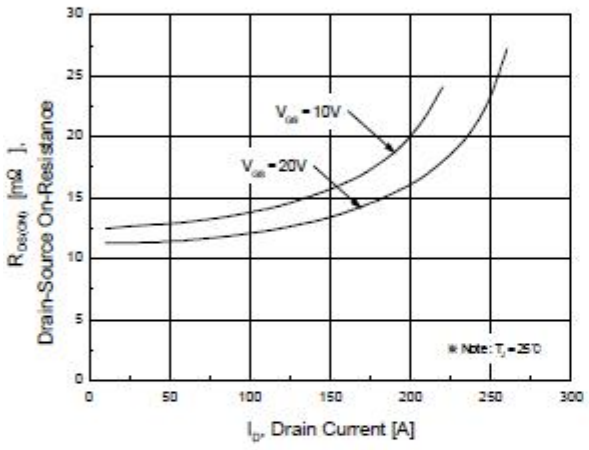


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

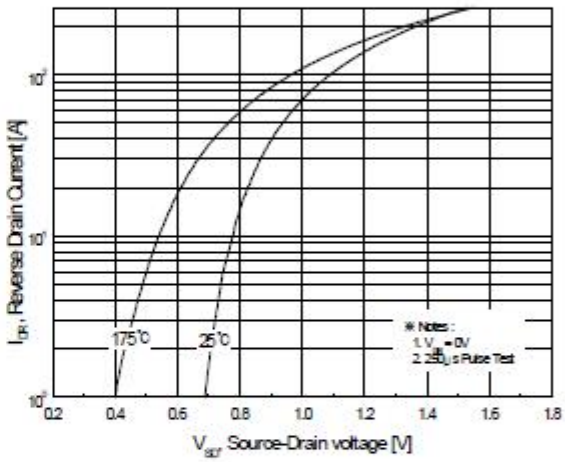


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

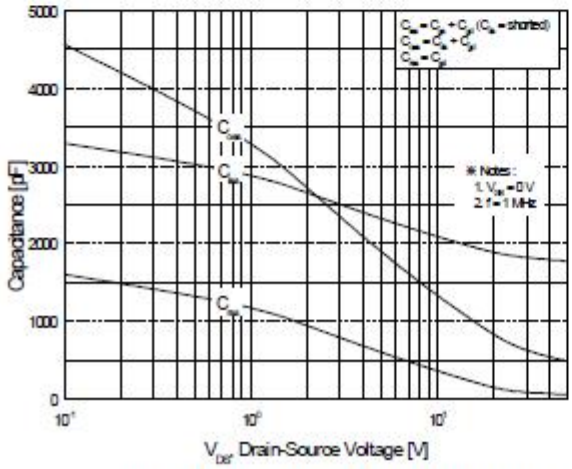


Figure 5. Capacitance Characteristics

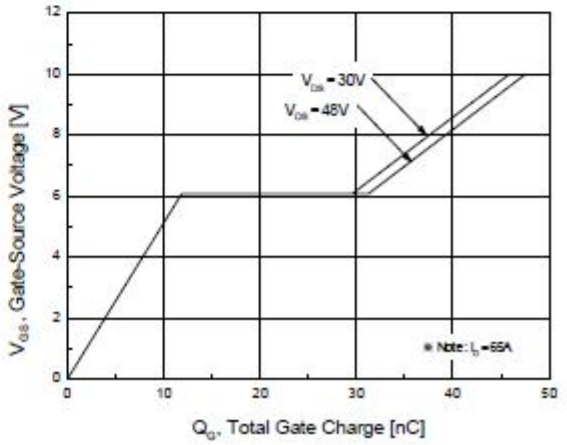


Figure 6. Gate Charge Characteristics

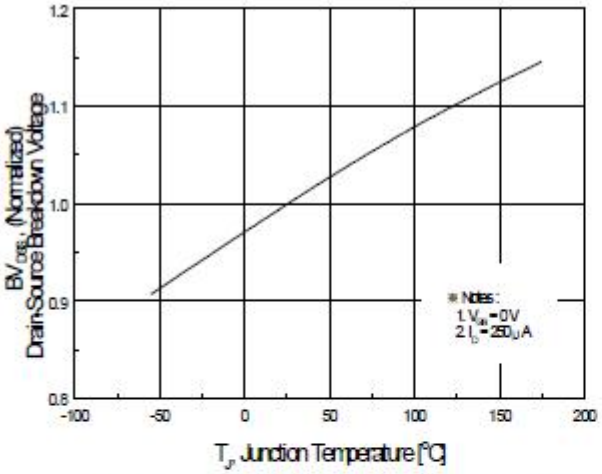


Figure 7. Breakdown Voltage Variation vs. Temperature

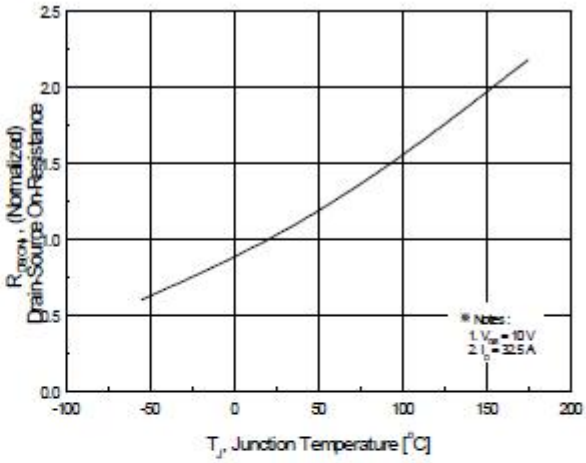


Figure 8. On-Resistance Variation vs. Temperature

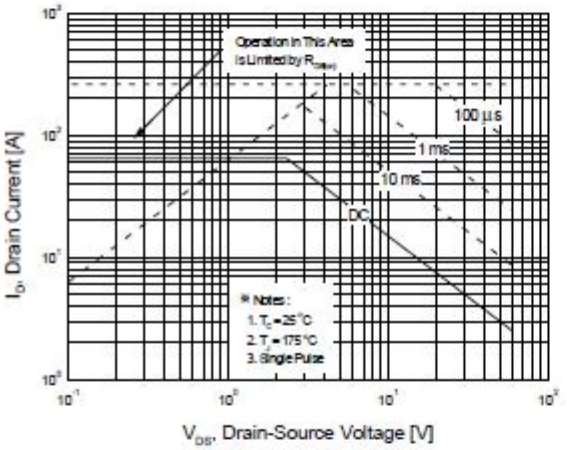


Figure 9. Maximum Safe Operating Area

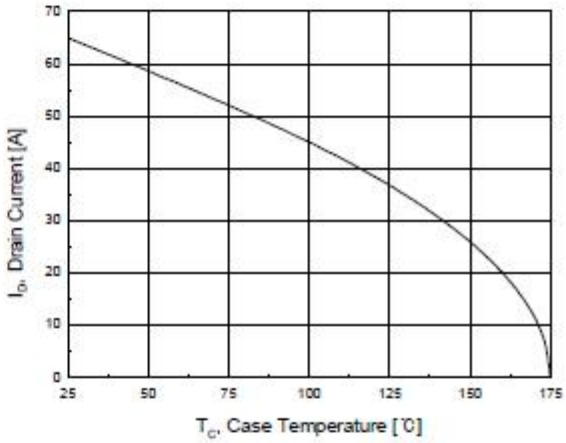


Figure 10. Maximum Drain Current vs. Case Temperature

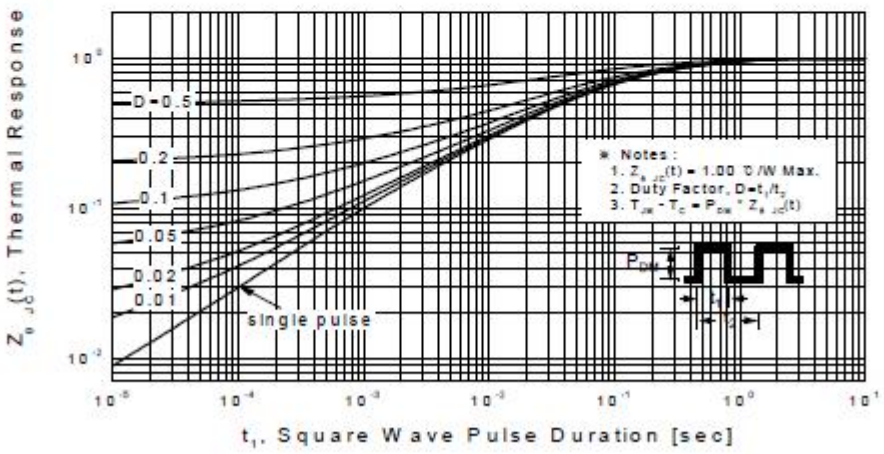
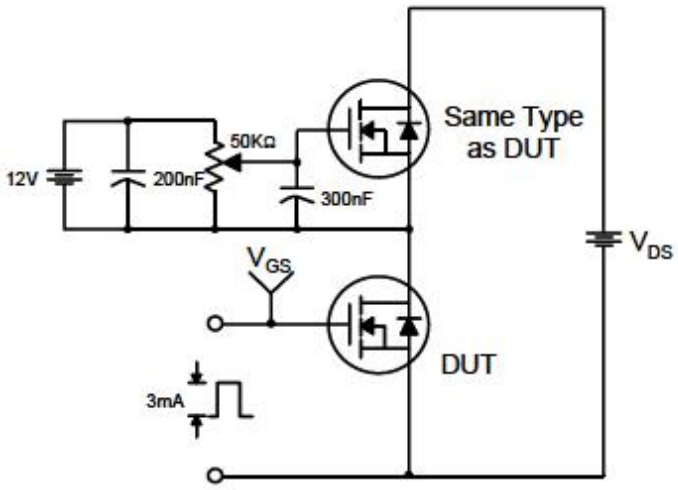
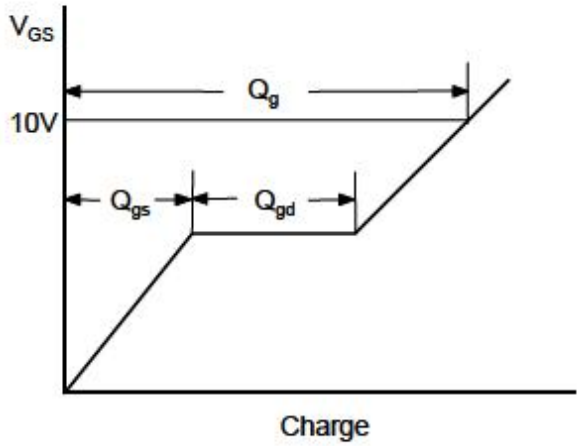


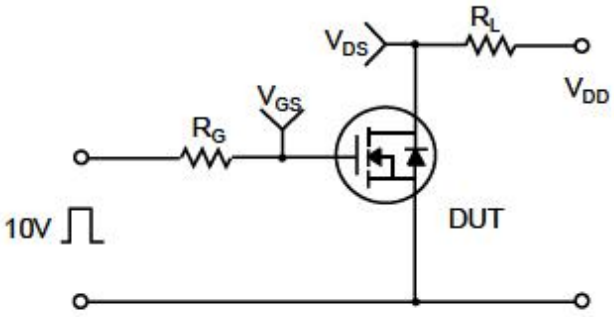
Figure 11. Transient Thermal Response Curve

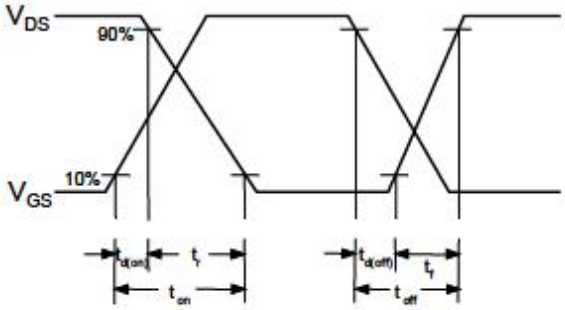
Gate Charge Test Circuit & Waveform



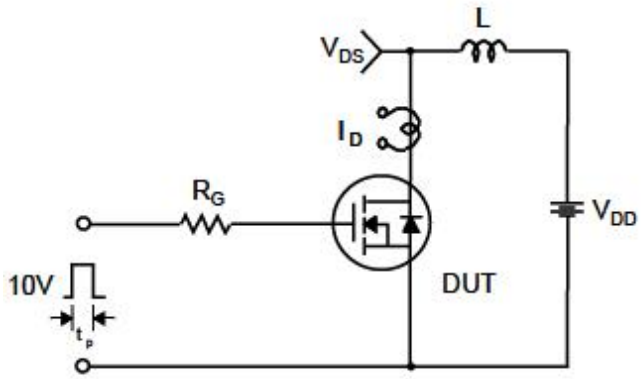


Resistive Switching Test Circuit & Waveforms

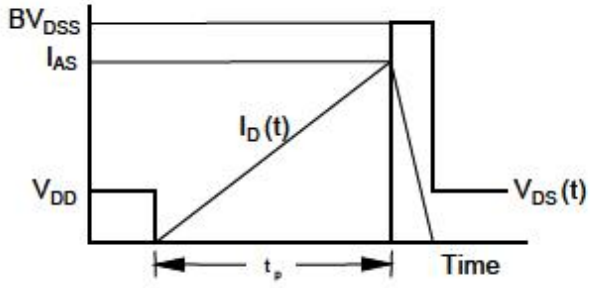




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms