



AO4406

N-Channel Enhancement Mode Field Effect Transistor

General Description

The AO4406/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device makes an excellent high side switch for notebook CPU core DC-DC conversion. AO4406 and AO4406L are electrically identical.

-RoHS Compliant

-AO4406L is Halogen Free

Features

V_{DS} (V) = 30V

I_D = 11.5A (V_{GS} = 10V)

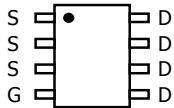
$R_{DS(ON)} < 14m\Omega$ (V_{GS} = 10V)

$R_{DS(ON)} < 16.5m\Omega$ (V_{GS} = 4.5V)

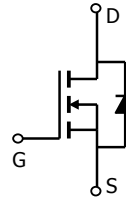
$R_{DS(ON)} < 26m\Omega$ (V_{GS} = 2.5V)

UIS TESTED!

Rg,Ciss,Coss,Crss Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^{AF}	I_D	11.5	A
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$		9.6	
Pulsed Drain Current ^B	I_{DM}	80	
Avalanche Current ^B	I_{AV}	25	A
Repetitive Avalanche Energy ^B L=0.3mH	E_{AV}	94	mJ
Power Dissipation	P_D	3	W
		2.1	
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{AF}	$R_{\theta JA}$	23	40	$^\circ\text{C/W}$
$t \leq 10s$				
Maximum Junction-to-Ambient ^A		48	65	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	12	16	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.8	1	1.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=12\text{A}$ $T_J=125^\circ\text{C}$		11.5 16	14 19.2	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$		13.5	16.5	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$, $I_D=8\text{A}$		19.5	26	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=10\text{A}$	25	38		S
V_{SD}	Diode Forward Voltage	$I_S=10\text{A}$, $V_{GS}=0\text{V}$		0.83	1	V
I_S	Maximum Body-Diode Continuous Current				4.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		1630	2300	pF
C_{oss}	Output Capacitance			201		pF
C_{rss}	Reverse Transfer Capacitance			142	200	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	0.4	0.8	1.8	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=4.5\text{V}$, $V_{DS}=15\text{V}$, $I_D=11.5\text{A}$	13.5	18	24	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			5.5		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=1.2\Omega$, $R_{GEN}=3\Omega$		4	6	ns
t_r	Turn-On Rise Time			5	7.5	ns
$t_{D(off)}$	Turn-Off DelayTime			32	50	ns
t_f	Turn-Off Fall Time			5	10	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=10\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		18.7	24	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=10\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		12.5	15	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

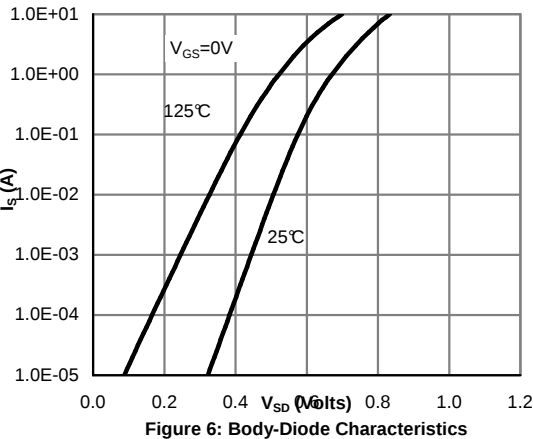
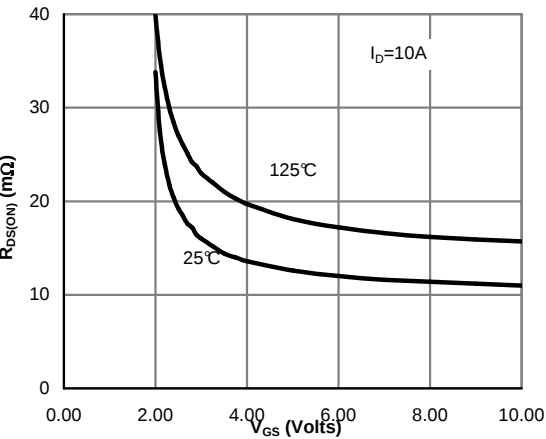
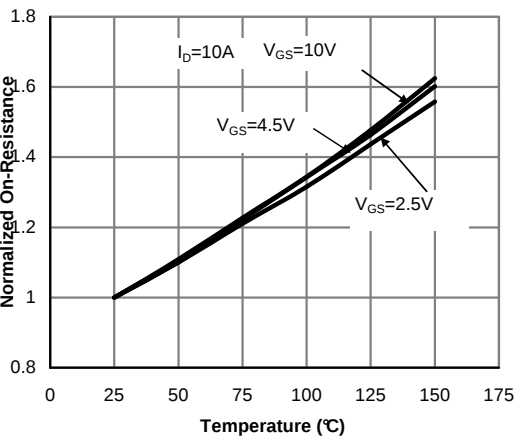
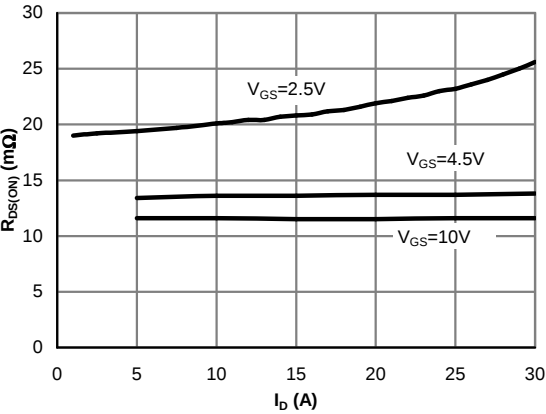
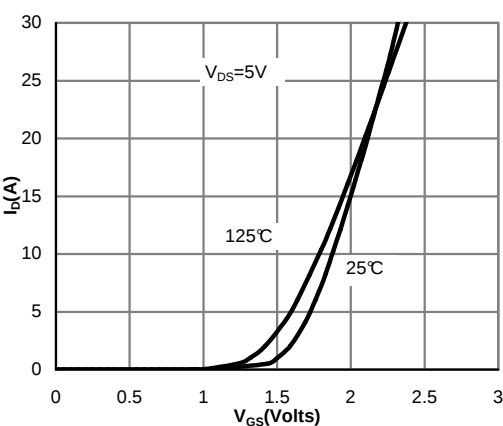
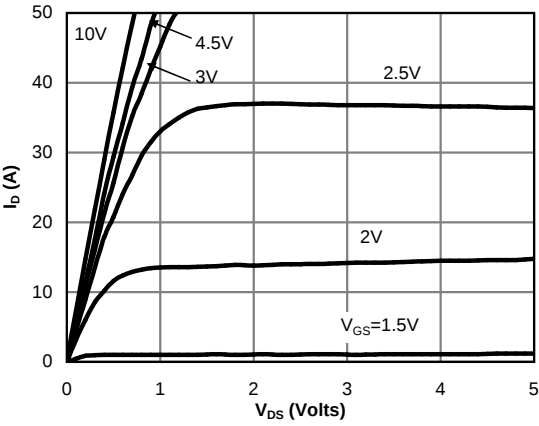
E: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $t \leq 10\text{s}$ junction to ambient thermal resistance rating.

Rev9: May 2011

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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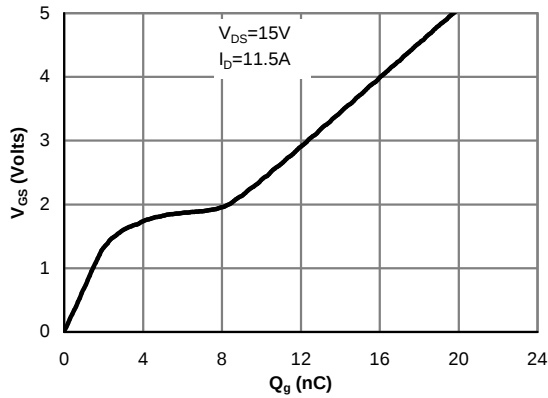


Figure 7: Gate-Charge Characteristics

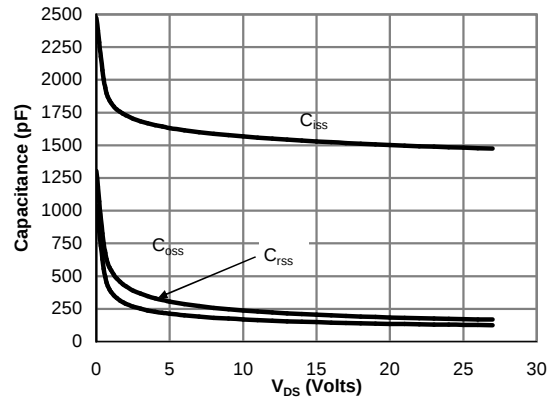


Figure 8: Capacitance Characteristics

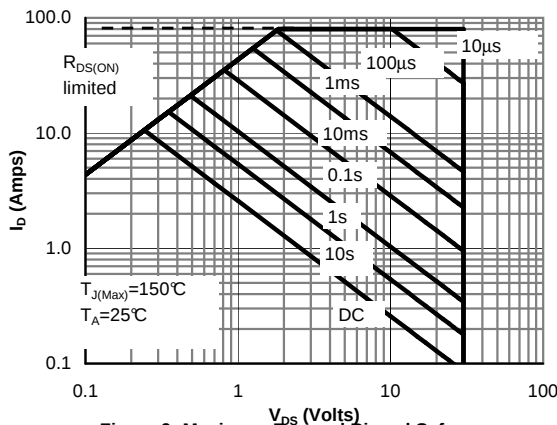


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

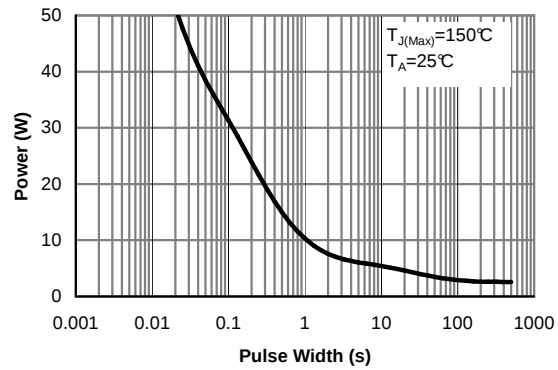


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

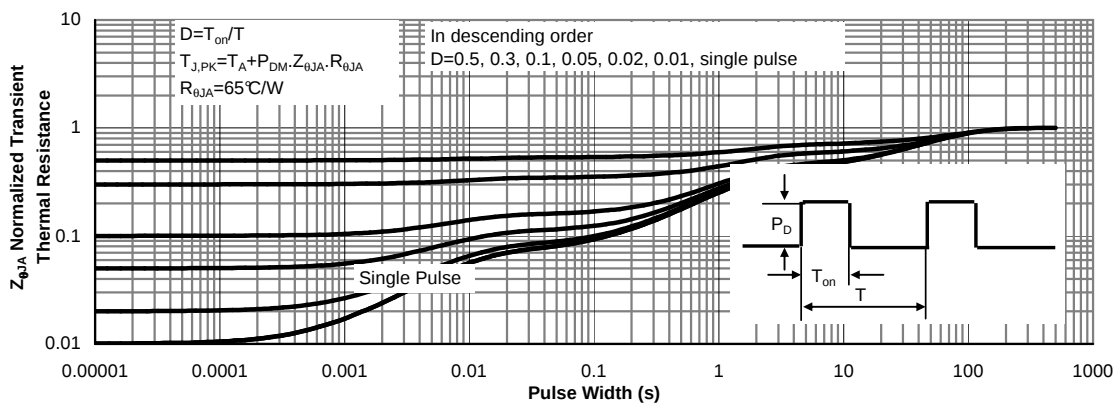
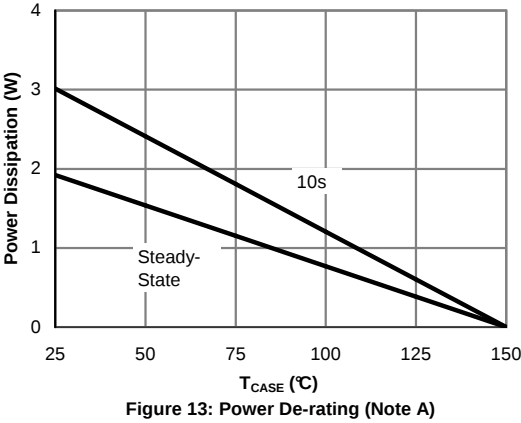
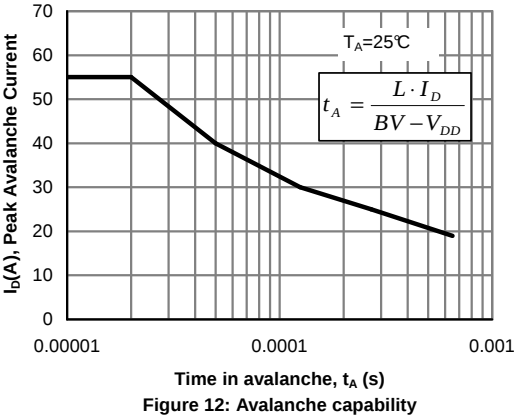
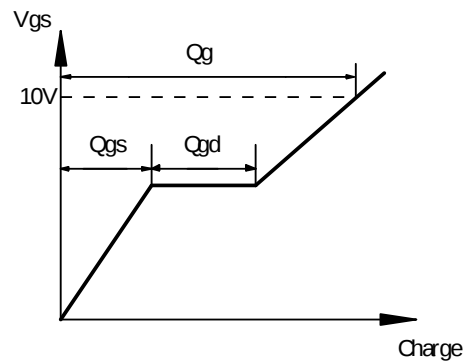
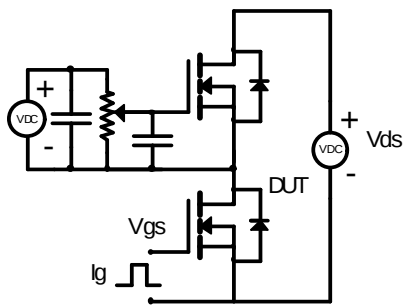


Figure 11: Normalized Maximum Transient Thermal Impedance

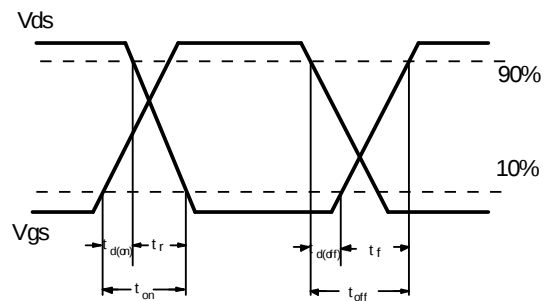
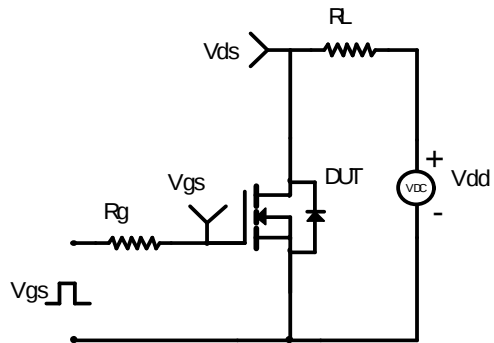
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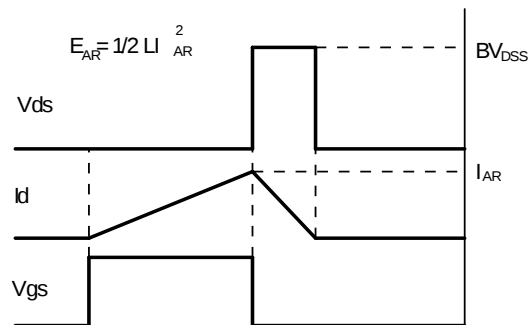
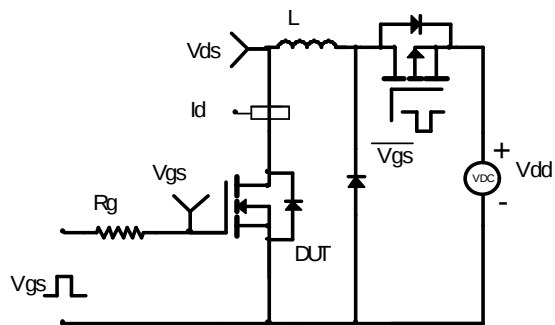
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

